My 40+ Year Journey from Mainframes to Smart Phones

Dileep Bhandarkar, Ph. D.
IEEE Fellow

The Stops Along My Journey

- 1970: B. Tech, Electrical Engineering
  - Indian Institute of Technology, Bombay
- 1973: PhD in Electrical Engineering
  - Carnegie Mellon University
  - Thesis: Performance Evaluation of Multiprocessor Computer Systems
- 4 years - Texas Instruments
  - Research on magnetic bubble & CCD memory, FT DRAM
- 17 years - Digital Equipment Corporation
  - Processor Architecture and Performance
- 12 years - Intel
  - Performance, Architecture, Strategic Planning
- 5.5 years - Microsoft
  - Distinguished Engineer, Data Center Hardware Engineering
- 5 months and counting – Qualcomm Technologies Inc
  - VP Technology

Birth of ISCA!

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My 15 Minutes of Fame!

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MARKOV CHAIN MODELS FOR ANALYZING MEMORY INTERFERENCE IN MULTIPROCESSOR COMPUTER SYSTEMS[1]

Dileep P. Bhandarkar[2]
Samuel H. Fuller
Carnegie-Mellon University
Pittsburgh, Pennsylvania

ABSTRACT

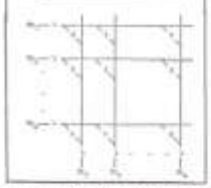
This paper discusses various analytical techniques for studying the extent of memory interference in a multiprocessor system with a crosspoint switch for processor-memory communication. Processor behavior is modelled as an ordered sequence of a memory request followed by an interval of processing time. The system is assumed to be bus bound; in other words, by the time the processor-memory bus completes servicing a processor's request the processor is ready to initiate another request and the memory module is ready to accept another request. The techniques discussed include discrete and continuous time Markov chain models as well as several approximate analytic methods.

1. INTRODUCTION

Carnegie-Mellon University is currently in the process of constructing a multiprocessor computer system (C.mmp) that will have up to 16 central processors (Pc's) sharing the same physical address space (4) and concern has been expressed about the performance of such a system with these many active processors. In addition to the processors, there is a set of memory modules that are able to operate independently; little would be gained if all the processors had to wait for service from a single memory module. Between the processors and the memory modules (Mp's) is a n by m switch. There are a number of ways of implementing the switch, but C.mmp employs a full n by m crosspoint switch as shown in Figure 1.1. Other multiprocessors, although limited to a smaller number of Pc's, also basically use a crosspoint switch, e.g. the Burroughs BBC1 and the Univac 1110. For further discussion of crosspoint switches, and a variety of other switching structures, see Bell and Newell (3).

Mathematical models of computer systems can be developed at various levels of abstraction. A large number of models for time-sharing systems consider a job as a basic unit (cf. 10), and in many models of multiprogrammed computer systems the block of instructions between I/O operations is taken as a basic unit (cf. 9). However, in this study a much more detailed

FIGURE 1.1
n×m Crossbar Switch



model is used to analyze interference as processors access individual words from the memory modules. Each processor's performance is measured by the number of memory accesses per unit time. The major contribution of this paper is a systematic method for a discrete Markov chain model. Other techniques described include Strecker's approximation (13), systems with exponentially distributed memory service time, and a diffusion approximation.

2. GENERAL MODELING ASSUMPTIONS

Due to the complexity of the problem, the most detailed behavior of memory interference in a multiprocessor system is difficult to model. We make the following assumptions with respect to the parameters that characterize the behavior of a Pc.

Instruction mix: In general, processor behavior varies for different instructions. However, in this paper differences in instructions are ignored. Processor behavior is modeled as an ordered sequence of a memory request followed by an interval of execution time. At this level of abstraction no distinction is made between the processing needed to decode an instruction and the processing corresponding to its execution. Thus, the processing time characterizing a Pc depicts only the aggregate behavior of the real Pc. Figure 2.1 depicts the actual and abstracted behaviors.

Processing time of Pc: The models discussed here assume that the multiprocessor systems are bus bound, i.e. the Pc is ready to initiate the next request and the Mp module is ready to accept the next request at the time the Pc-Mp bus recovers from the current access. The analysis is also applicable to multiprocessor systems in which the effective processing time, tp, is equal to the memory rewrite time, tw.

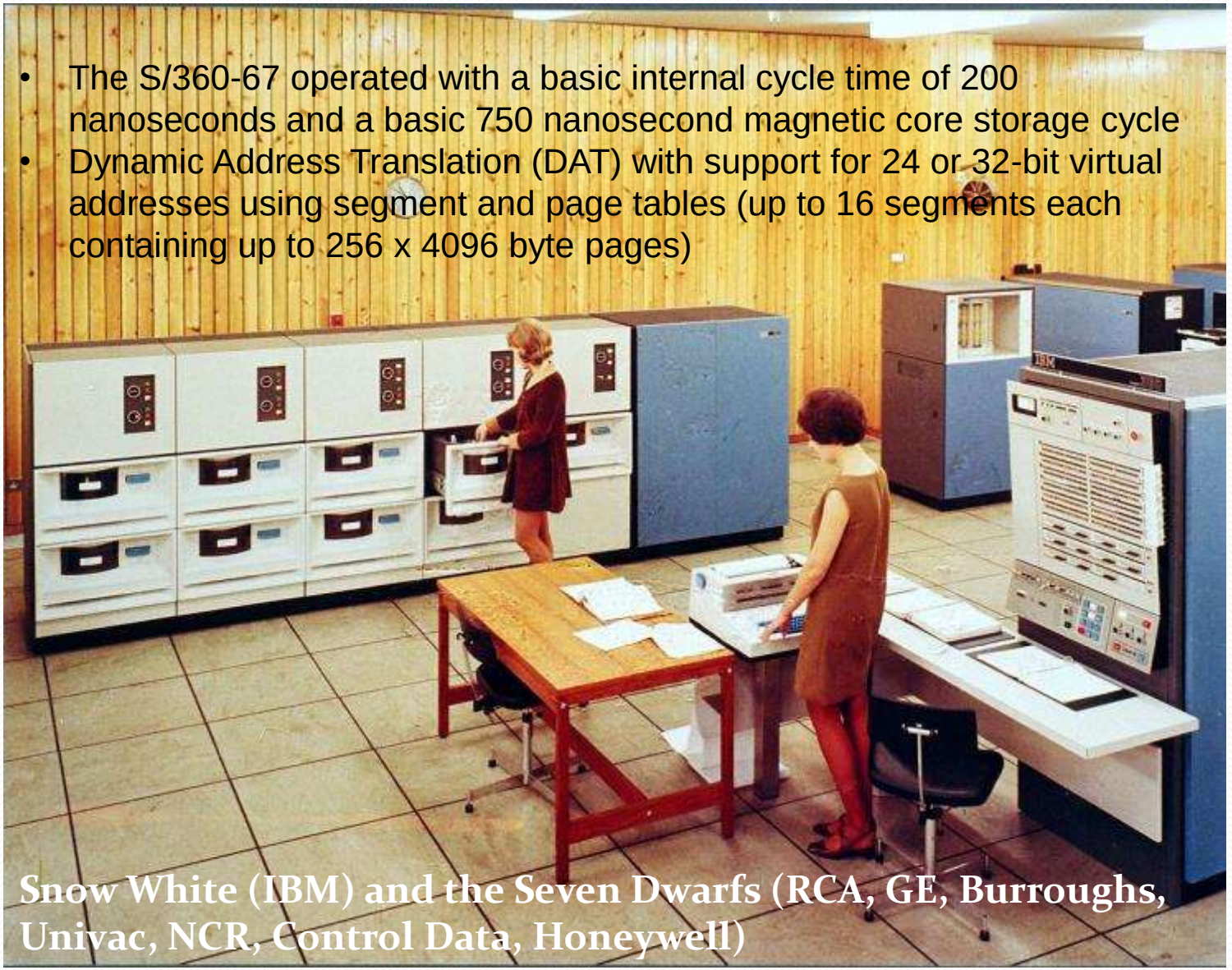
Access pattern of a Pc: This is the sequence of memory locations accessed by the Pc. In this study serial correlation between successive memory accesses

[1] This work was supported by the Advanced Research Projects Agency of the Office of the Secretary of Defense (DAHC15-73-C-0074) and is monitored by the Air Force Office of Scientific Research.

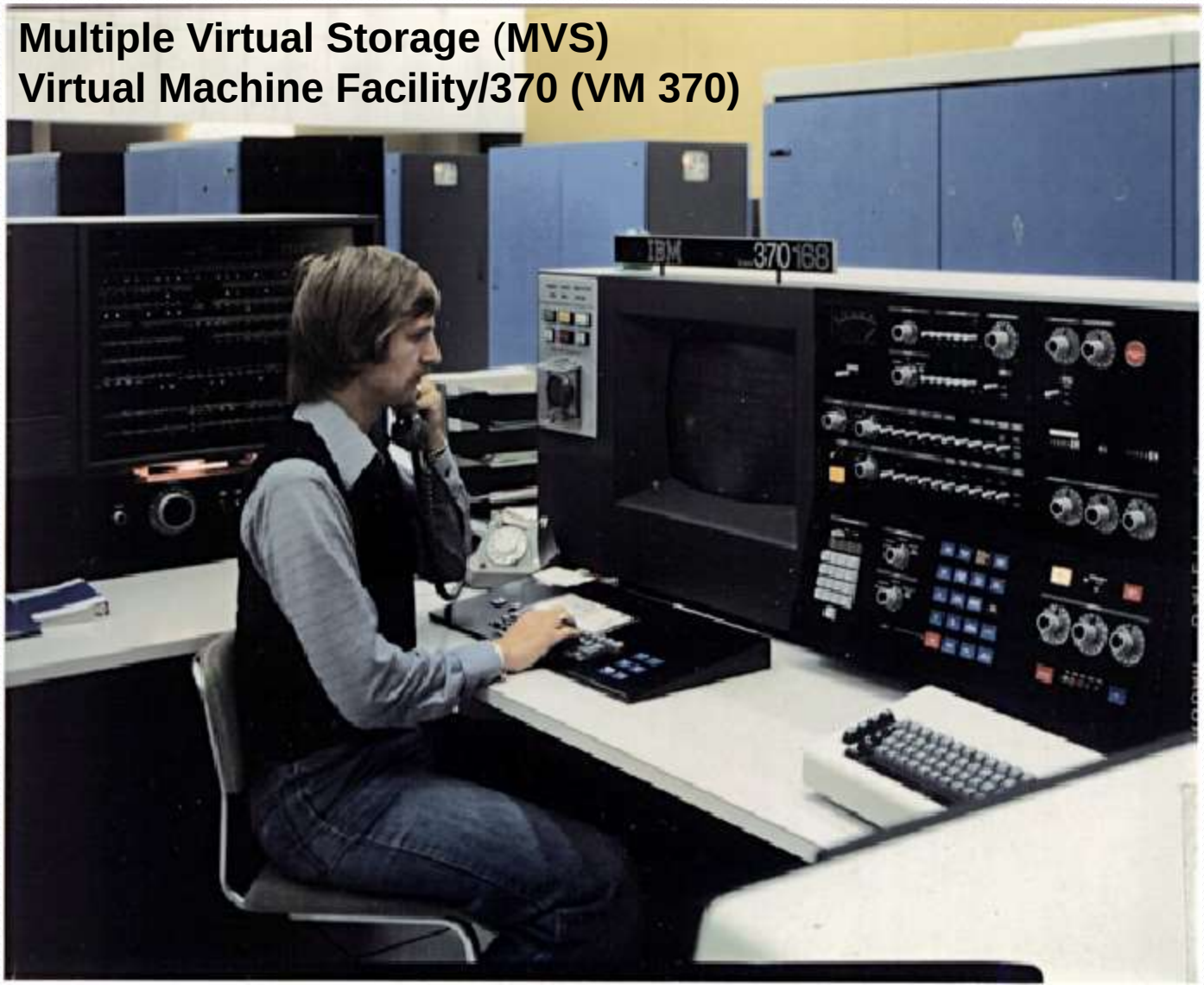
[2] D. P. Bhandarkar is now with Texas Instruments Inc., Dallas, Texas.

[3] We use the PMS notation of Bell and Newell (3) in this report to describe hardware organization.

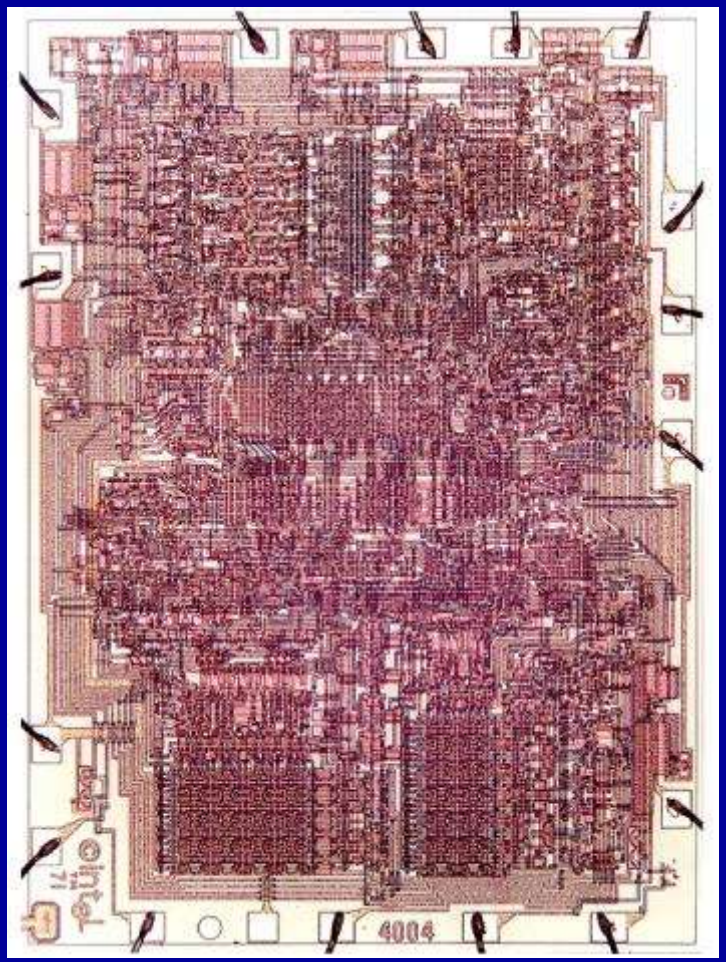
IBM 360/67 at CMU in 1970



IBM 370/168 – circa 1974



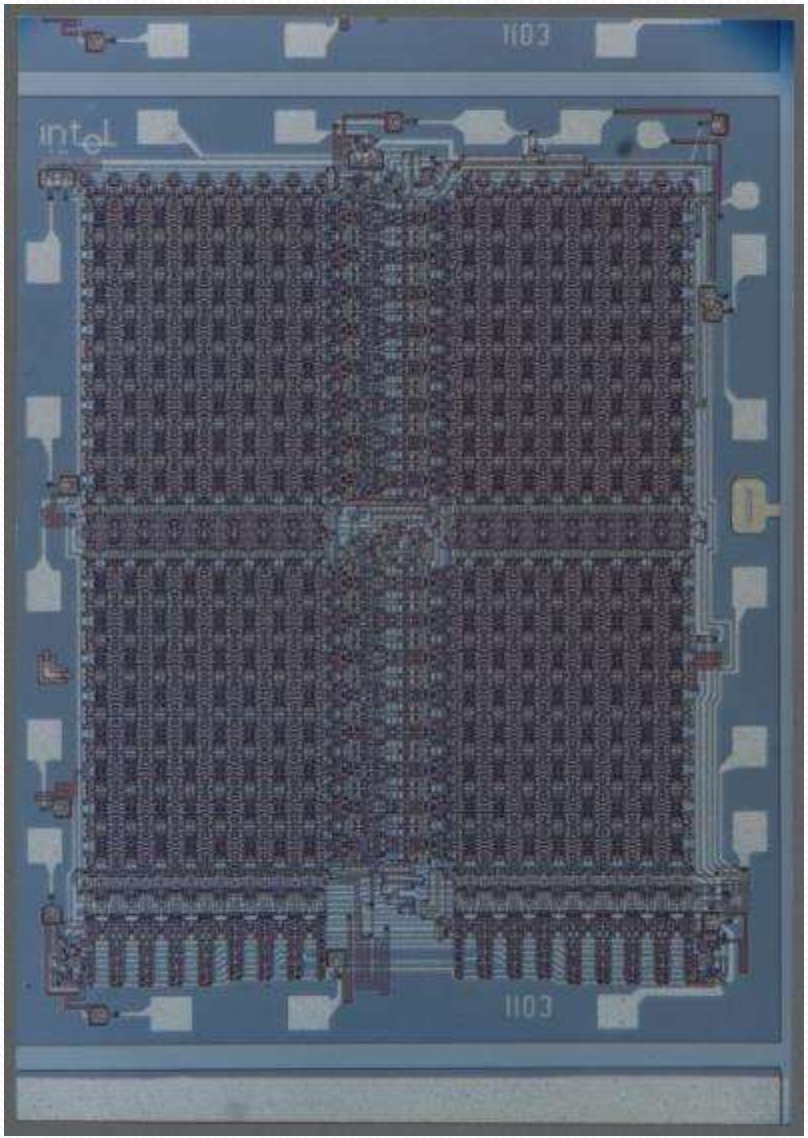
1971: 4004 Microprocessor



- The 4004 was Intel's first microprocessor. This breakthrough invention powered the Busicom calculator and paved the way for embedding intelligence in inanimate objects as well as the personal computer.

Introduced November 15, 1971
108 KHz, 50 KIPs , 2300 10μ transistors

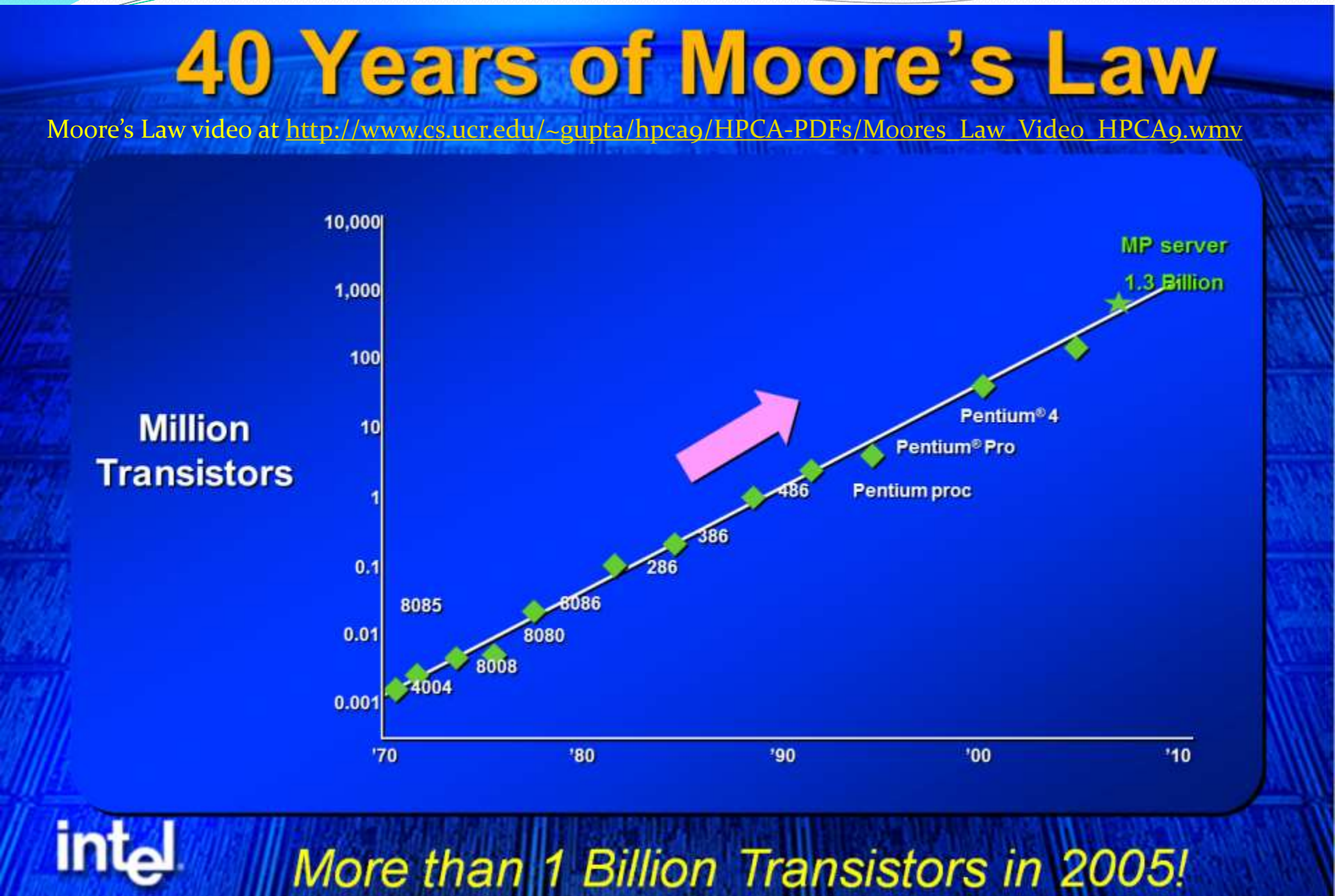
1971: 1K DRAM



Intel® 1103 DRAM Memory

- Intel delivered the 1103 to 14 of the 18 leading computer manufacturers.
- Since the production costs of the 1103 were much lower than the costs of a core memory or a 1101 the 1103 could establish within the market rapidly, became the world's best selling memory chip and was finally responsible for the obsolescence of magnetic core memory.

From 2300 to >1Billion Transistors



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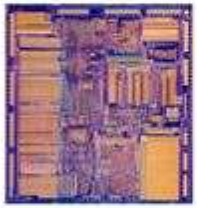
COMPUTER HISTORY MUSEUM

The Silicon Engine:
A Timeline of Semiconductors in Computers

MOORE'S LAW

"Transistor density on integrated circuits doubles about every two years." *

1950s	1960s	1970s	1980s	1990s	2000s
Silicon Transistor	TTL Quad Gate	8-bit Microprocessor	32-bit Microprocessor	32-bit Microprocessor	64-bit Microprocessor
					
1 Transistor	**16 Transistors**	**4500 Transistors**	**275,000 Transistors**	**3,100,000 Transistors**	**592,000,000 Transistors**

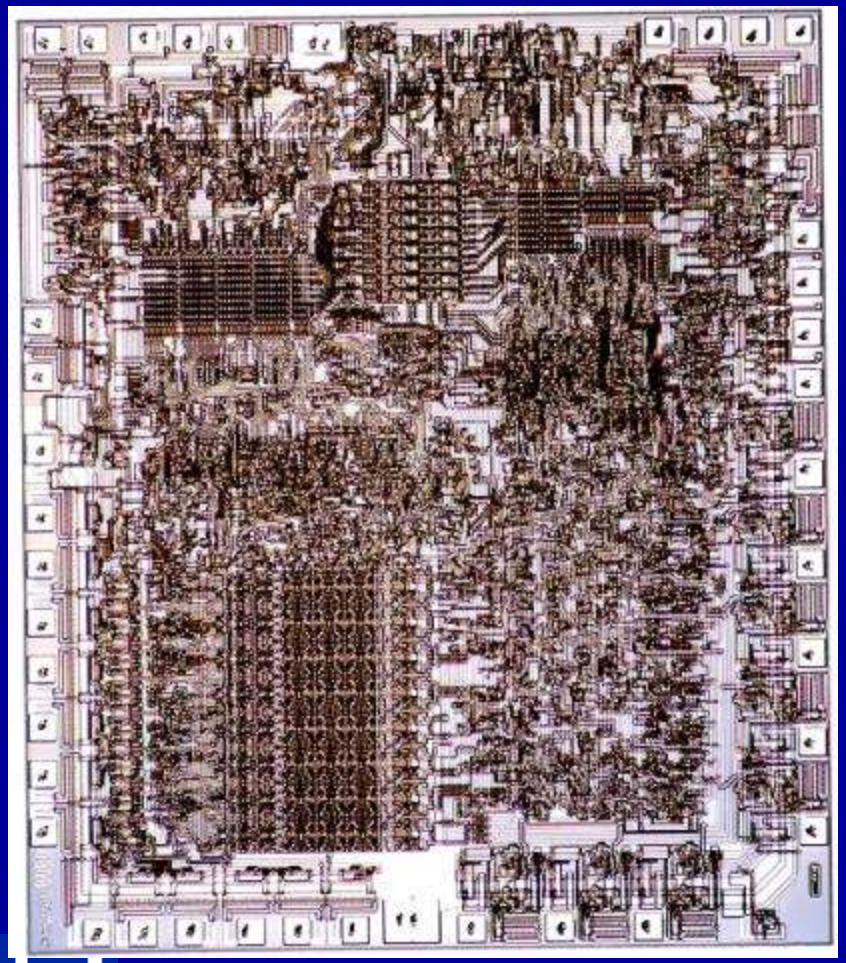
Microelectronic silicon computer "chips" have grown in capability from a single transistor in the 1950s to hundreds of millions of transistors per chip on today's microprocessor and memory devices. From the first documented semiconductor effect in 1833 to the transition from transistors to integrated circuits in the 1960s and 70s, this website explores key milestones in the development of these extraordinary engines that power the computing and communications revolution of the information age.

*Source: "Moore's Law: Raising the Bar" (Intel Corporation 2005)

Photo credits: Fairchild Camera and Instrument Corporation, Intel Corporation (Note that images are not to scale)

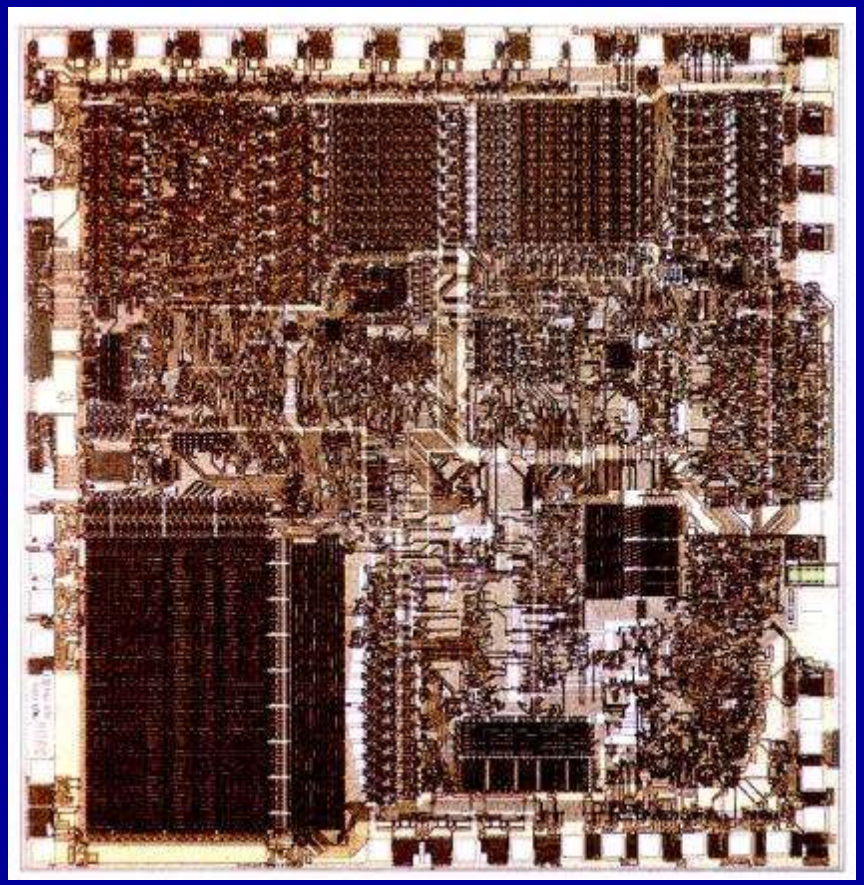
1958
Integrated Circuit

1974: 8080 Microprocessor



- The 8080 became the brains of the first personal computer--the Altair, allegedly named for a destination of the Starship *Enterprise* from the *Star Trek* television show. Computer hobbyists could purchase a kit for the Altair for $395. Within months, it sold tens of thousands, creating the first PC back orders in history.

1978: 8086-8088 Microprocessor



- A pivotal sale to IBM's new personal computer division made the 8088 the brains of IBM's new hit product--the IBM PC. The 8088's success propelled Intel into the ranks of the *Fortune 500*, and *Fortune* magazine named the company one of the "Business Triumphs of the Seventies."

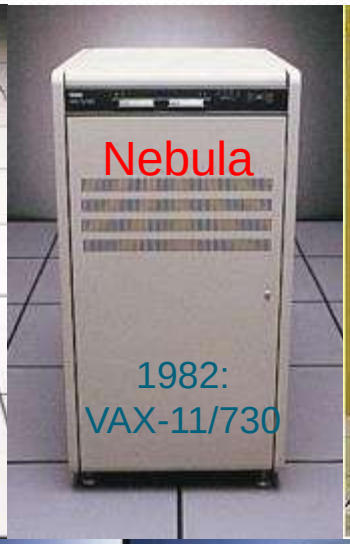
DEC PDP-11

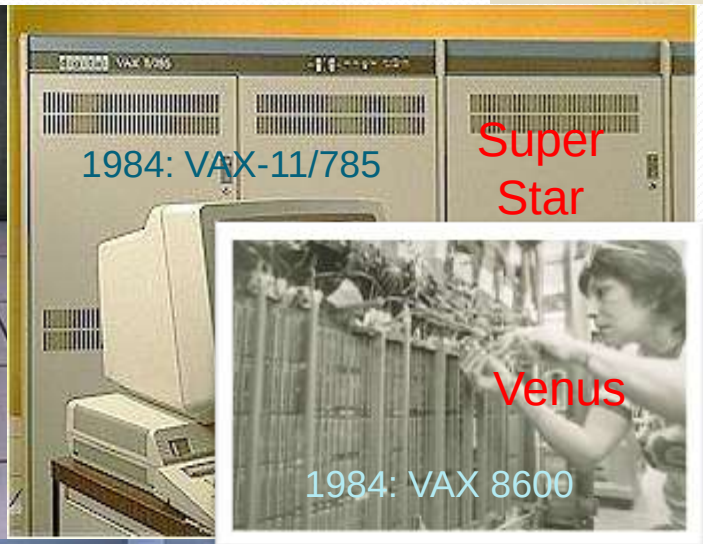
1977: VAX-11/780 – STAR is Born!

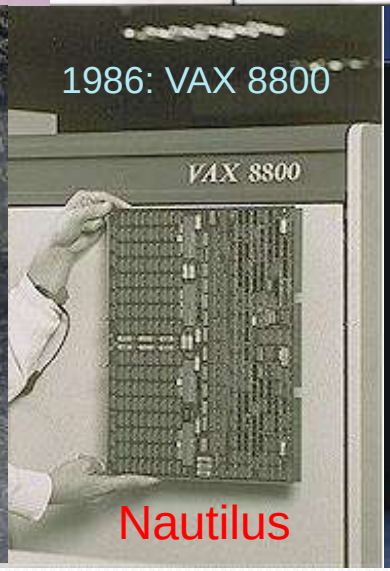
Evolution of VAX Architecture:

- MicroVAX Subset
- VAXvector Extensions

VAX Family: 1977 - 1992





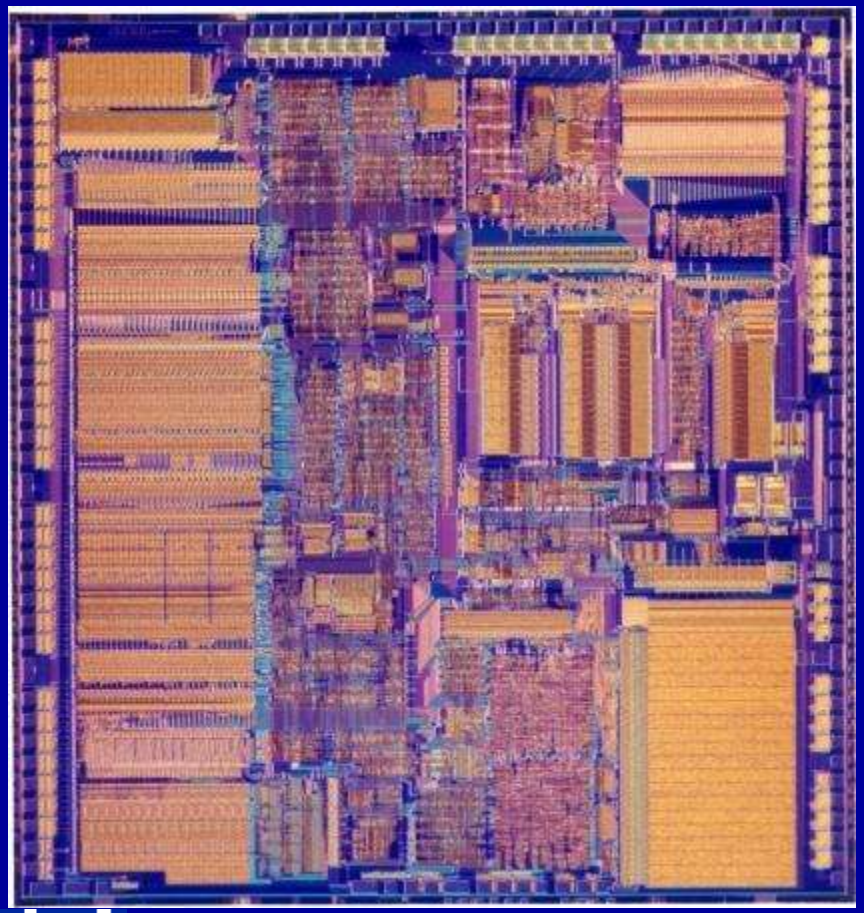


1981: First IBM PC

The IBM Personal Computer ("PC")

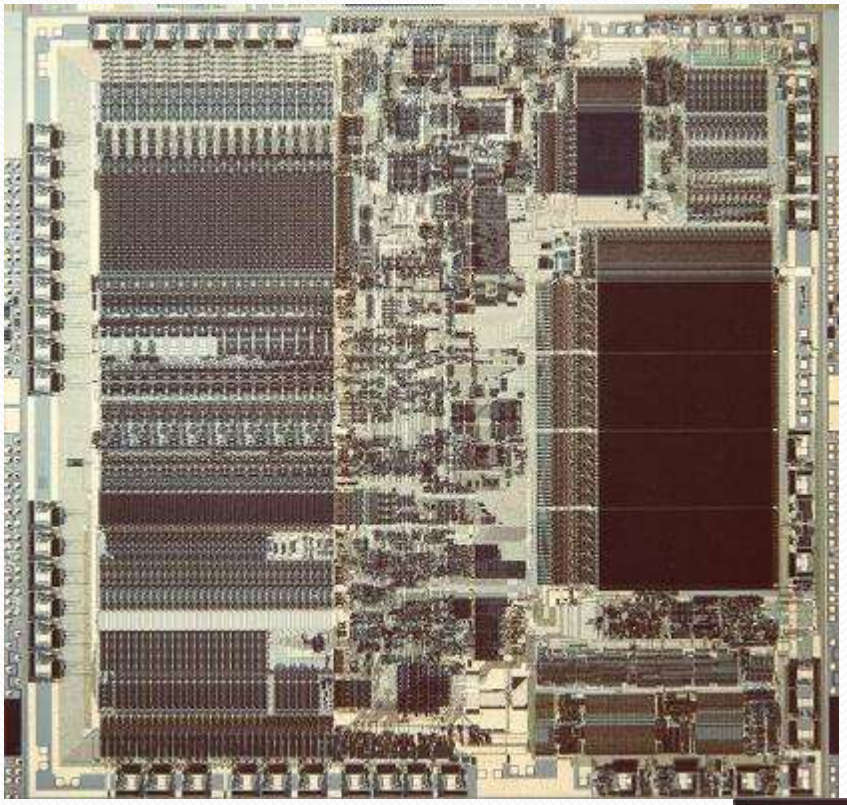
- PC-DOS Operating System
- Microsoft BASIC programming language, which is built-in and included with every PC.
- Typical system for home use with a memory of 64K bytes, a single diskette drive and its own display, was priced around $3,000.
- An expanded system for business with color graphics, two diskette drives, and a printer cost about $4,500.

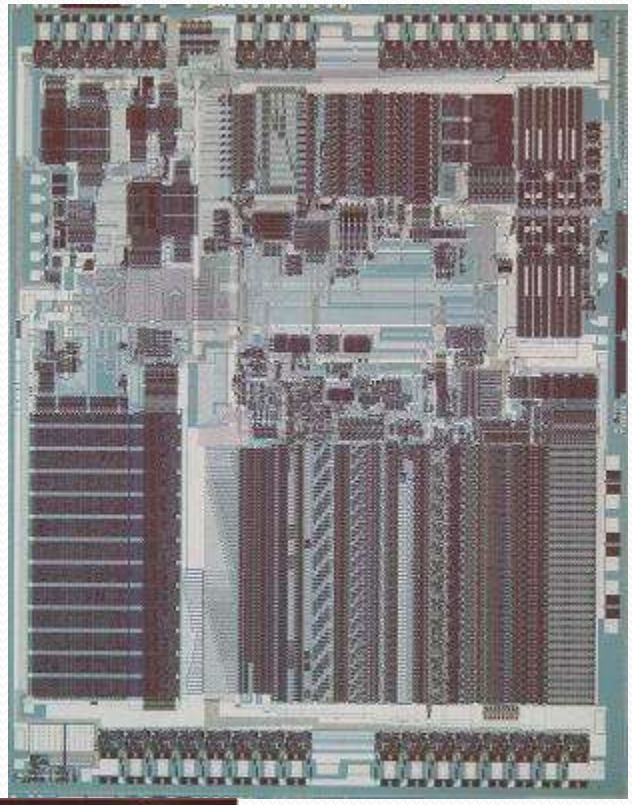
1985: Intel386™ Microprocessor



- The Intel386™ microprocessor featured 275,000 transistors--more than 100 times as many as the original 4004. It was a Intel's first 32-bit chip.

1985: MicroVAX-II

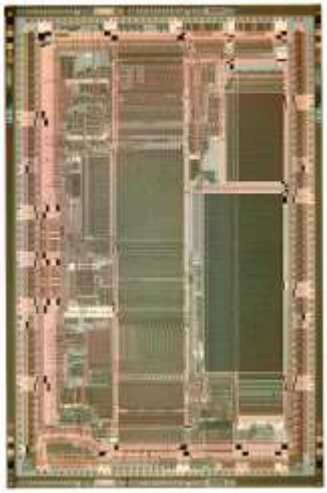




The **MicroVAX- I** (*Seahorse*), introduced in October 1984, was the first VAX computers to use VLSI Technology.

RISC vs CISC WARS

- Sun SPARC
- MIPS R2000, R3000, R4000, R6000, R10000
- PA-RISC
- IBM Power and Power PC
- DEC Alpha 21064, 21164, 21264



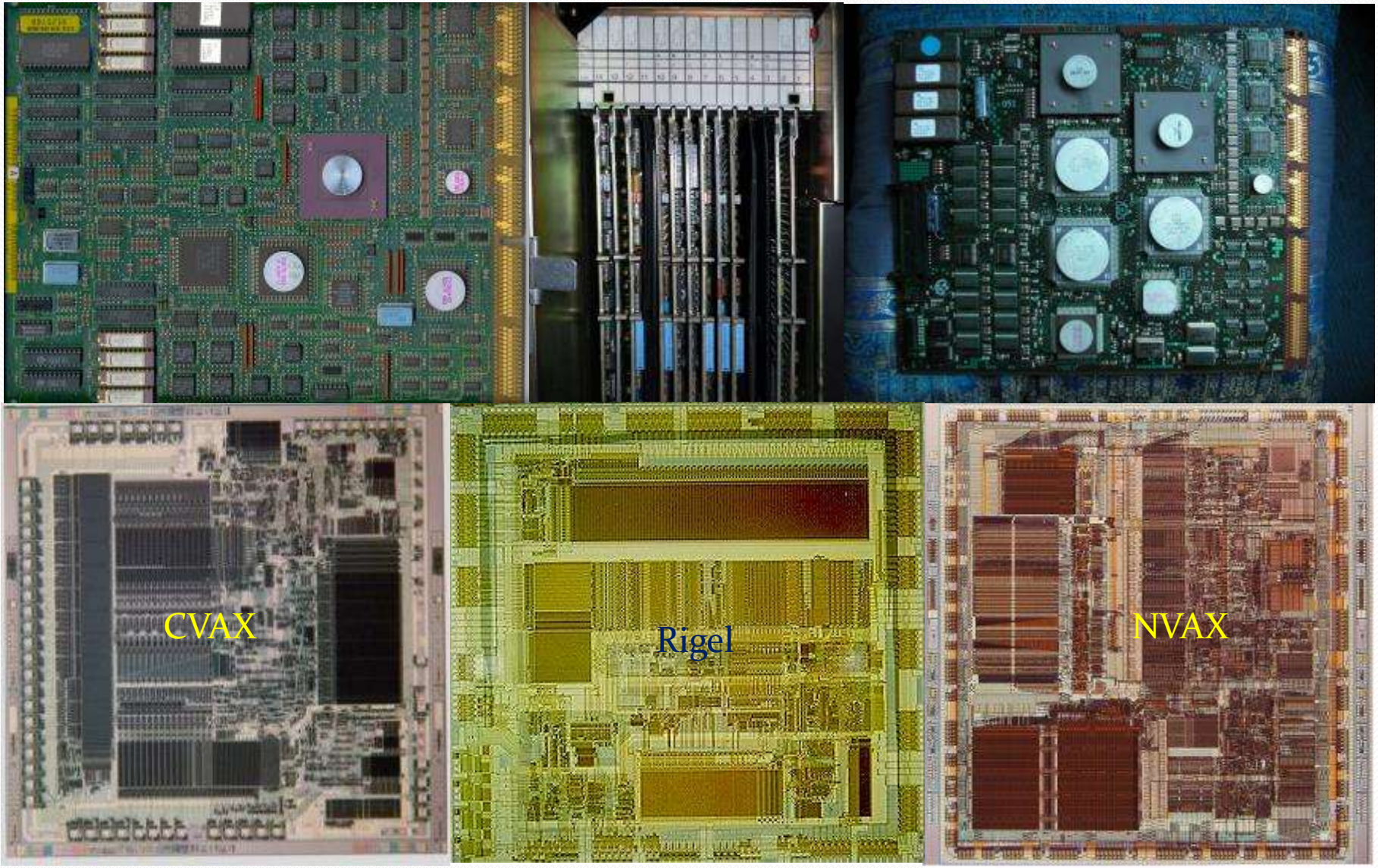
In 1987, the introduction of RISC processors based on Sun's SPARC architecture spawned the now famous RISC vs CISC debates. DEC cancelled PRISM in 1988. RISC processors from MIPS, IBM (Power, Power PC), and HP (PA-RISC) started to gain market share. This forced Digital to adopt MIPS processors in 1989, and later introduce Alpha in 1992.

High Performance Issue Oriented Architecture

D. Bhandarkar, D. Orbits, R. Witek, W. Cardoza, D. Cutler†

Digital Equipment Corporation

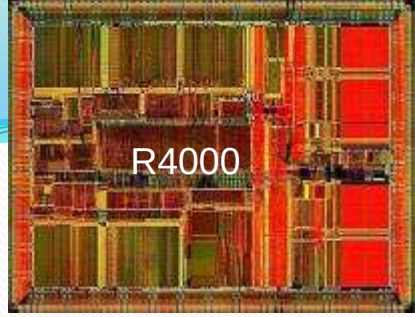
1988-1992: VAX 6000 Series



1989: VAX 9000 - The Age of Aquarius

The Beginning of the End of VAX

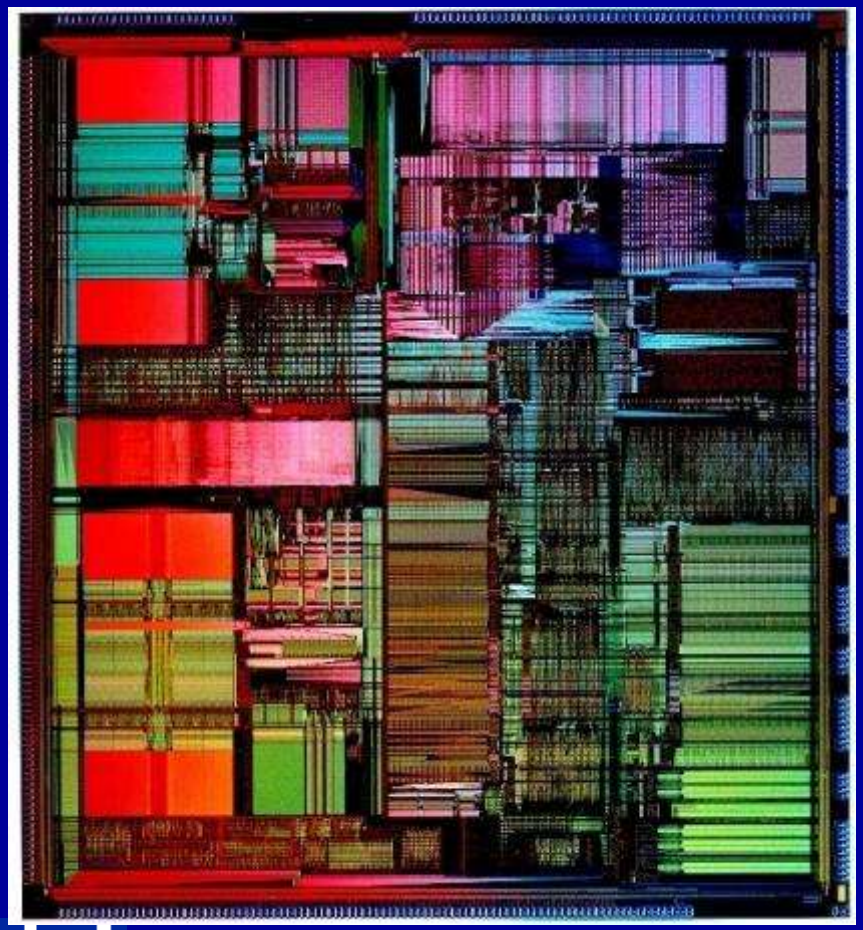
1991: ACE Initiative



- The Advanced Computing Environment (ACE) was defined by an industry consortium in the early 1990s to be the next generation commodity computing platform, the successor to personal computers based on Intel's 32-bit x86 instruction set architecture.
- The consortium was announced on the 9th of April 1991 by MIPS Computer Systems, Digital Equipment Corporation, Compaq, Microsoft, and the Santa Cruz Operation.
- At the time it was widely believed that RISC-based systems would maintain a price/performance advantage over the x86 systems.
- The environment standardized on the MIPS architecture and two operating systems: SCO UNIX with Open Desktop and what would become Windows NT (originally named OS/2 3.0).
- The Advanced RISC Computing (ARC) document was produced to give hardware and firmware specifications for the platform.
- When the initiative started, MIPS R3000 RISC based systems had substantial performance advantage over Intel 80486 and original 60 MHz Pentium chips .
- MIPS R4000 schedule and performance slipped and Intel updated the Pentium design to 90 MHz in the next semiconductor process generation and the MIPS performance advantage slipped away.

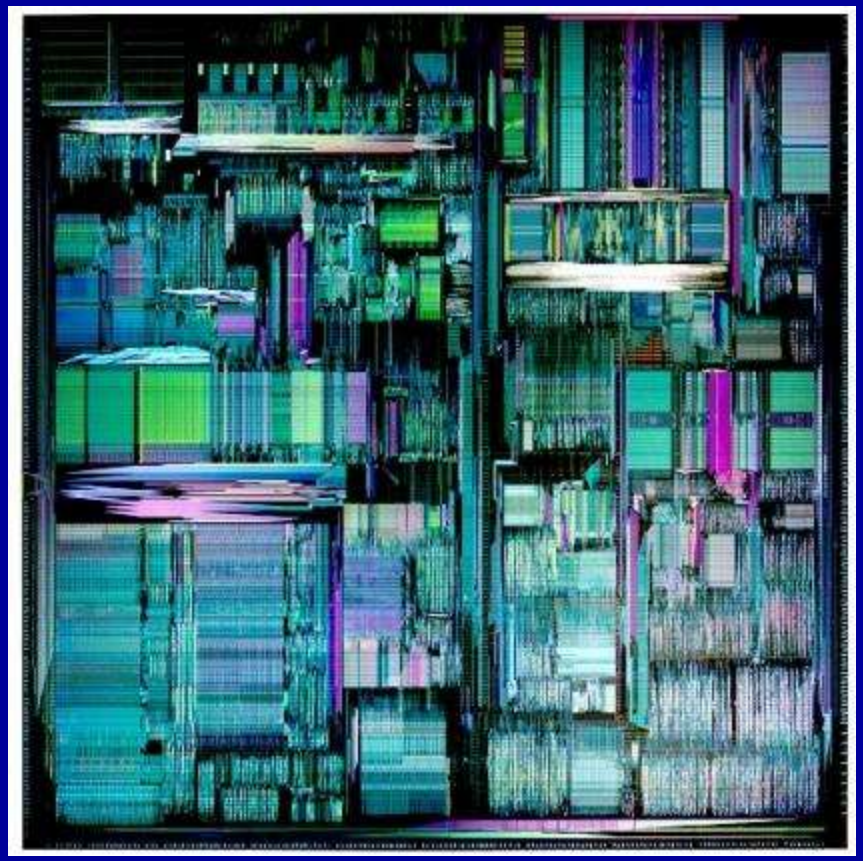
Strategy without Execution is Doomed!

1993: Intel® Pentium® Processor



- The Intel Pentium® processor allowed computers to more easily incorporate "real world" data such as speech, sound, handwriting and photographic images. The Intel Pentium brand, mentioned in the comics and on television talk shows, became a household word soon after introduction.
- 22 March 1993
- 66 MHz
- 3.1 M transistors
- 0.8µ

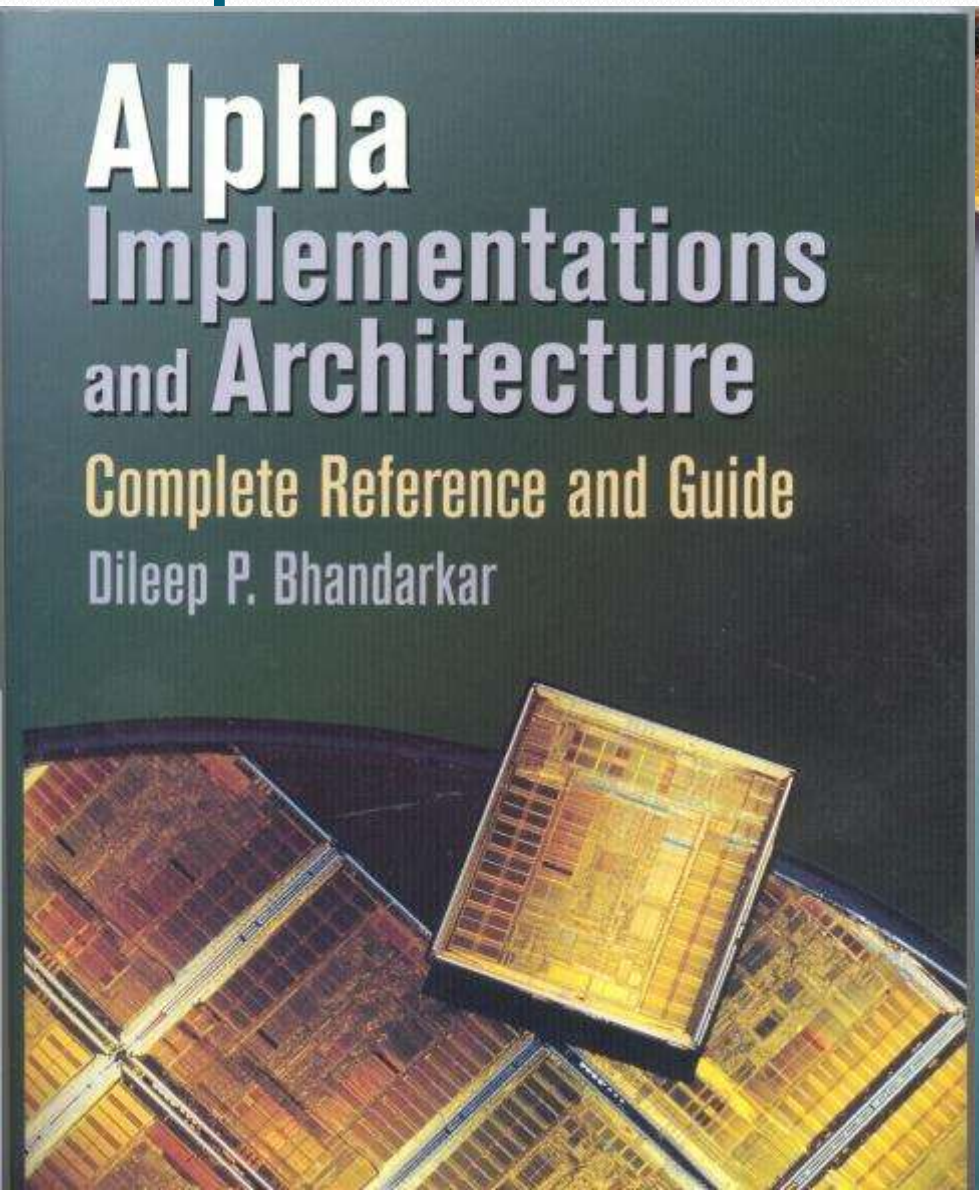
1995: Intel® Pentium® Pro Processor

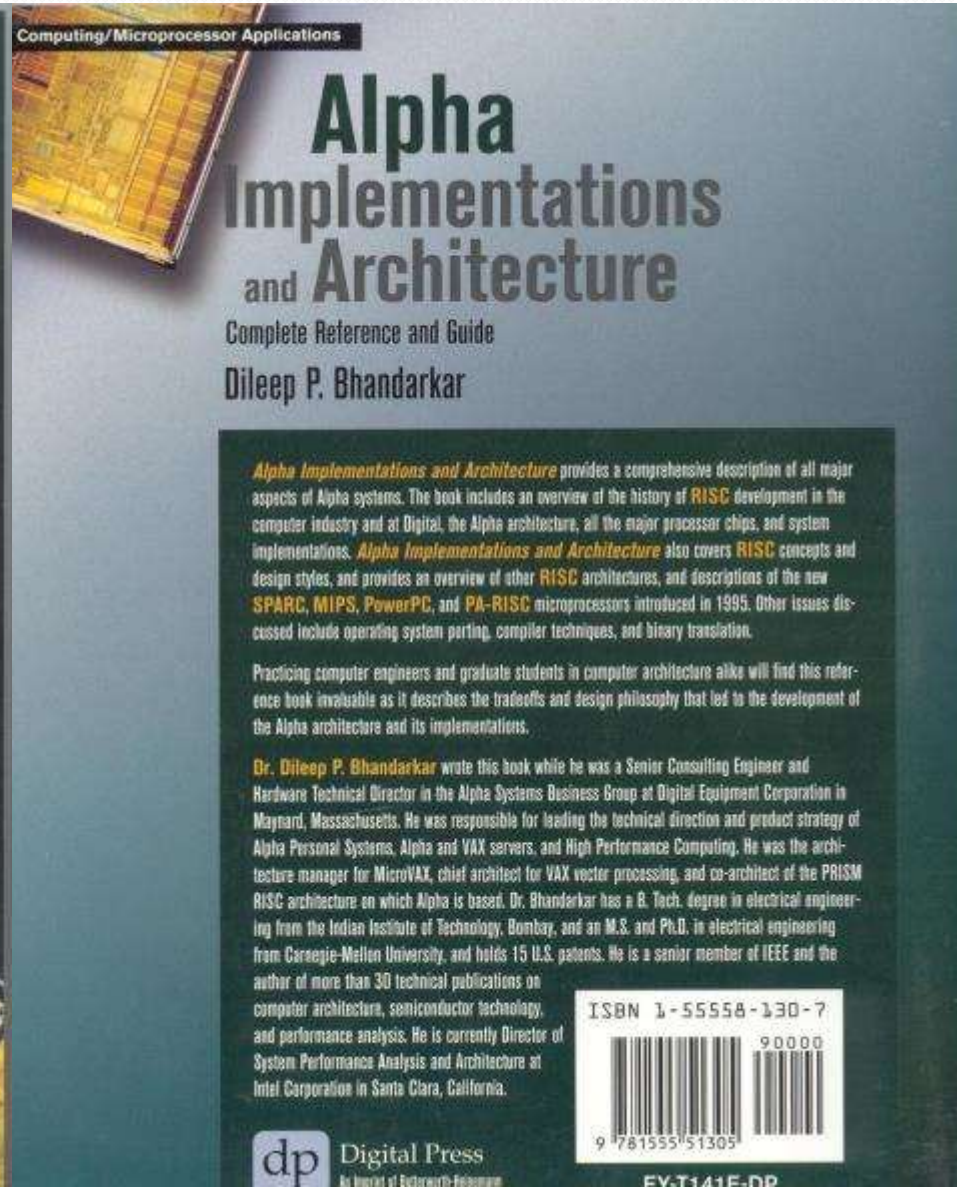


- Intel® Pentium® Pro processor was designed to fuel 32-bit server and workstation applications. Each Intel® Pentium Pro processor was packaged together with a second speed-enhancing cache memory chip. The powerful Pentium® Pro processor boasts 5.5 million transistors.
- 1 November 1995
- 200 MHz
- 0.35µ
- 1st x86 to implement out of order execution.

The RISC Killer!

Alpha was Too Little Too Late!





A Tale of 2 Chips

RISC versus CISC: A Tale of Two Chips

Dileep Bhandarkar
Intel Corporation
Santa Clara, California, USA

Abstract

This paper compares an aggressive RISC and CISC implementation built with comparable technology. The two chips are the Alpha® 21164 and the Intel Pentium® Pro processor. The paper presents performance comparisons for industry standard benchmarks and uses performance counter statistics to compare various aspects of both designs.

Introduction

In 1991, Bhandarkar and Clark published a paper comparing an example implementation from the RISC and CISC architectural schools (a MIPS® M/2000 and a Digital VAX® 8700) on nine of the ten SPEC89 benchmarks. The organizational similarity of these machines provided an opportunity to examine the purely architectural advantages of RISC. That paper showed that the resulting advantage in cycles per program ranged from slightly under a factor of 2 to almost a factor of 4, with a geometric mean of 2.7. This paper attempts yet another comparison of a leading RISC and CISC implementation, but using chips designed with comparable semiconductor technology. The RISC chip chosen for this study is the Digital Alpha 21164 [Edmondson95]. The CISC chip is the Intel Pentium® Pro processor [Colwell95]. The results should not be used to draw sweeping conclusions about RISC and CISC in general. They should be viewed as a snapshot in time. Note that performance is also determined by the system platform and compiler used.

Chip Overview

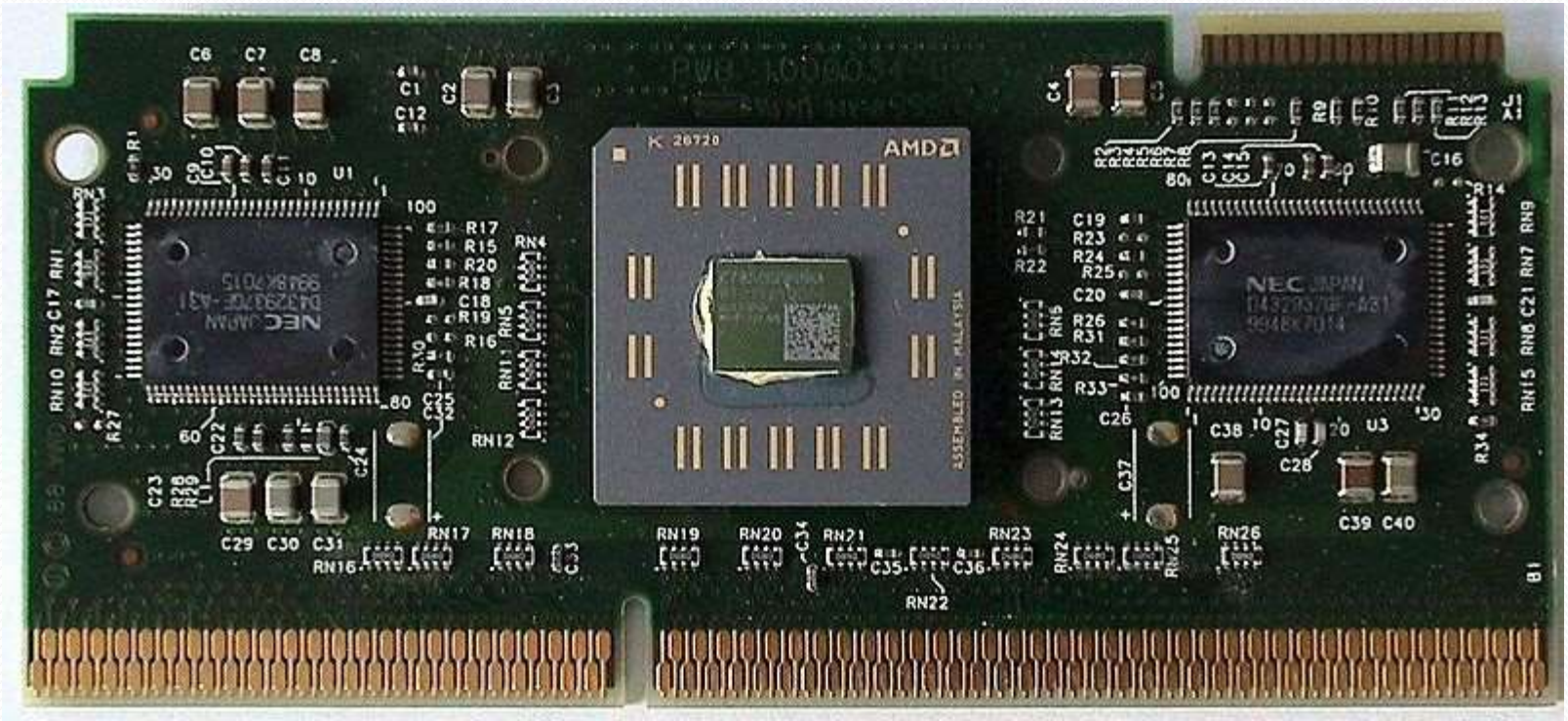
Table 1 shows the major characteristics of the two chips. Both chips are implemented in around 0.5µ technology and the die size is comparable. The design approach is quite different, but both represent state of the art implementations that achieved the highest performance for RISC and CISC architectures respectively at the time of their introduction.

Table 1 Chip Comparison

	Alpha 21164	Pentium® Pro Processor
Architecture	Alpha	IA-32
Clock Speed	300 MHz	150 MHz
Issue Rate	Four	Three
Function Units	four	five
Out of order issue	no	yes
Rename Registers	none	40
On-chip Cache	8 KB data 8KB instr 96 KB Level 2	8 KB data 8KB instr
Off chip cache	4 MB	256 KB
Branch History Table	2048 entries, 2-bit history	512 entries, 4-bit history
Transistors		
Logic	1.8 million	4.5 million
Total	9.3 million	5.5 million
VLSI Process	CMOS	BiCMOS
Min. Geometry	0.5 µ	0.6 µ
Metal Layers	4	4
Die Size	298 mm^2	306 mm^2
Package	499 pin PGA	387 pin PGA
Power	50 W	20 W incl cache
First Silicon	Feb. 94	4Q 94
Volume Parts	1Q 95	4Q 95
SPECint92/95	341/7.43	245/6.08
SPECfp92/95	513/12.4	220/5.42
SYSmark/NT	529	497

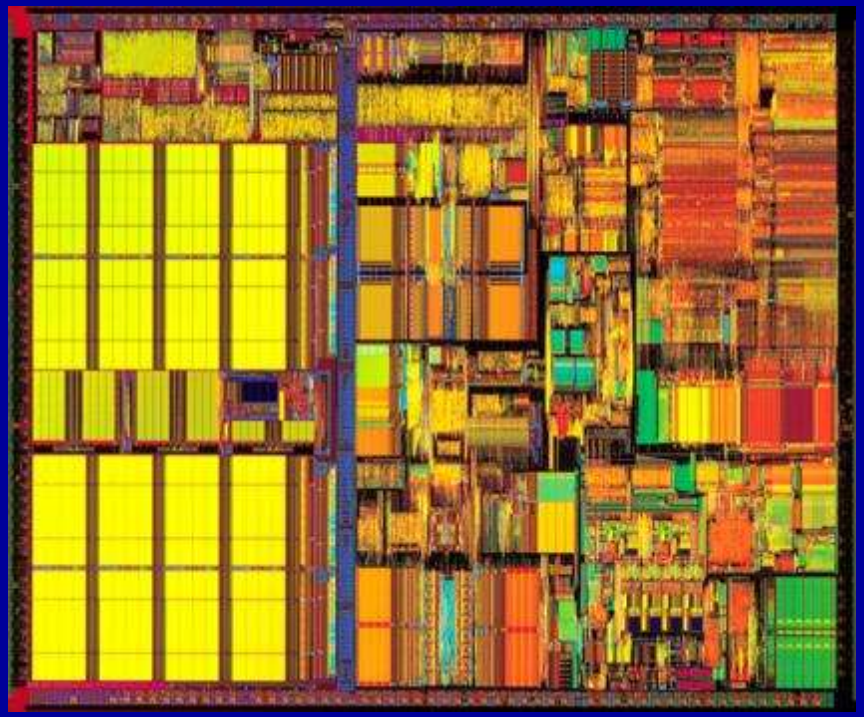
The 21164 is a quad issue superscalar design that implements two levels of caches on chip, but does not implement out of order execution. The Pentium® Pro processor implements dynamic execution using an out-of-order, speculative execution engine, with register renaming of integer, floating point and flags variables. Consequently, even though the die size is comparable, the total transistor count is quite different for the two chips. The aggressive design of the Pentium Pro processor is much more logic intensive; and logic transistors are less dense. The on-chip 96 KB L2 cache of the 21164 inflates its transistor count. Even though the Alpha 21164 has an on-chip L2 cache, most systems use a 2 or 4 MB board level cache to achieve their performance goal.

1999: AMD Athlon



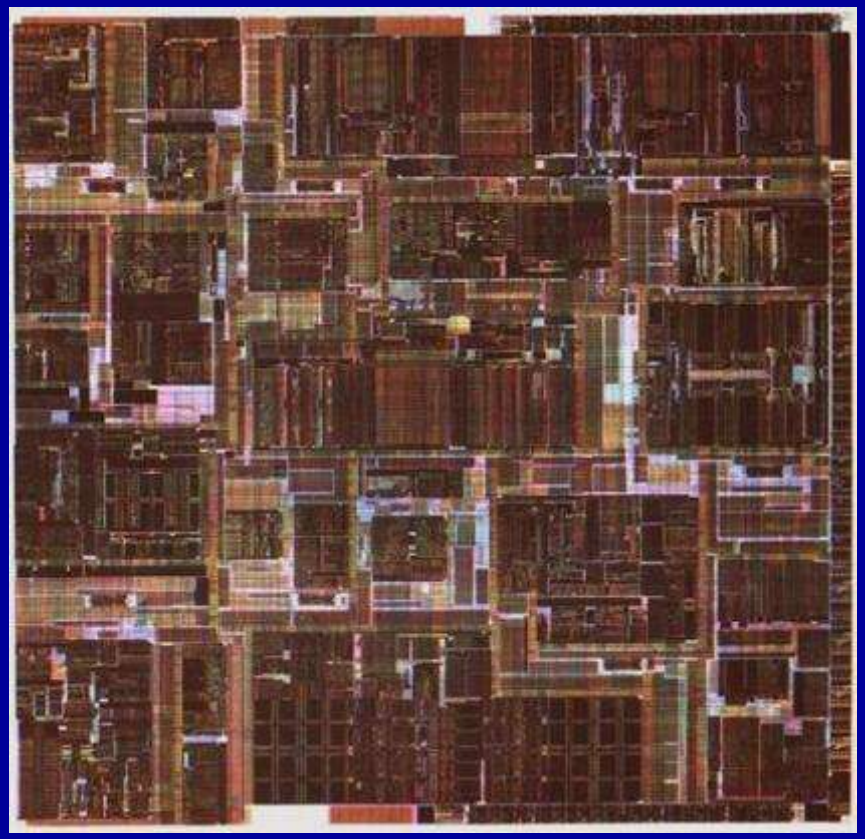
Won the Race to 1 GHz

1999: Intel® Pentium® III Processor – 0.18µ



- 25 Oct 1999
- Integrated 256KB L2 cache
- 733 MHz
- 28 M transistors
- First Intel microprocessor to hit 1 GHz on 8-Mar-2000, a few days after AMD Athlon!

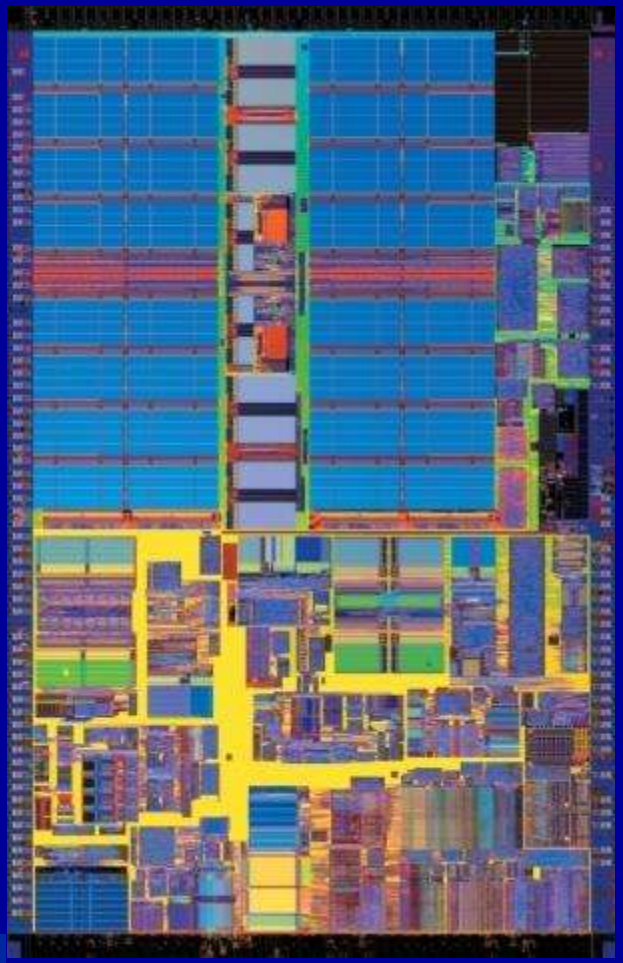
2001: Intel® Itanium™ Processor



- The Itanium™ processor is the first in a family of 64-bit products from Intel. Designed for high-end, enterprise-class servers and workstations, the processor was built from the ground up with an entirely new architecture based on Intel's Explicitly Parallel Instruction Computing (EPIC) design technology. May 2001
- 800 MHz
- 25M transistors
- 0.18µ
- External L3 cache

IT AIN'T PENTIUM !!!

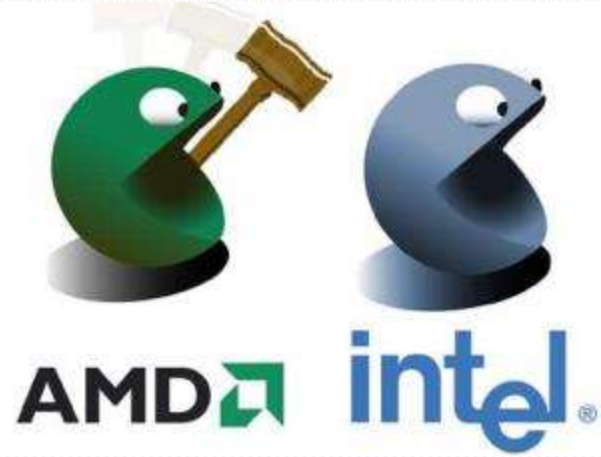
2003: Intel® Pentium® M Processor

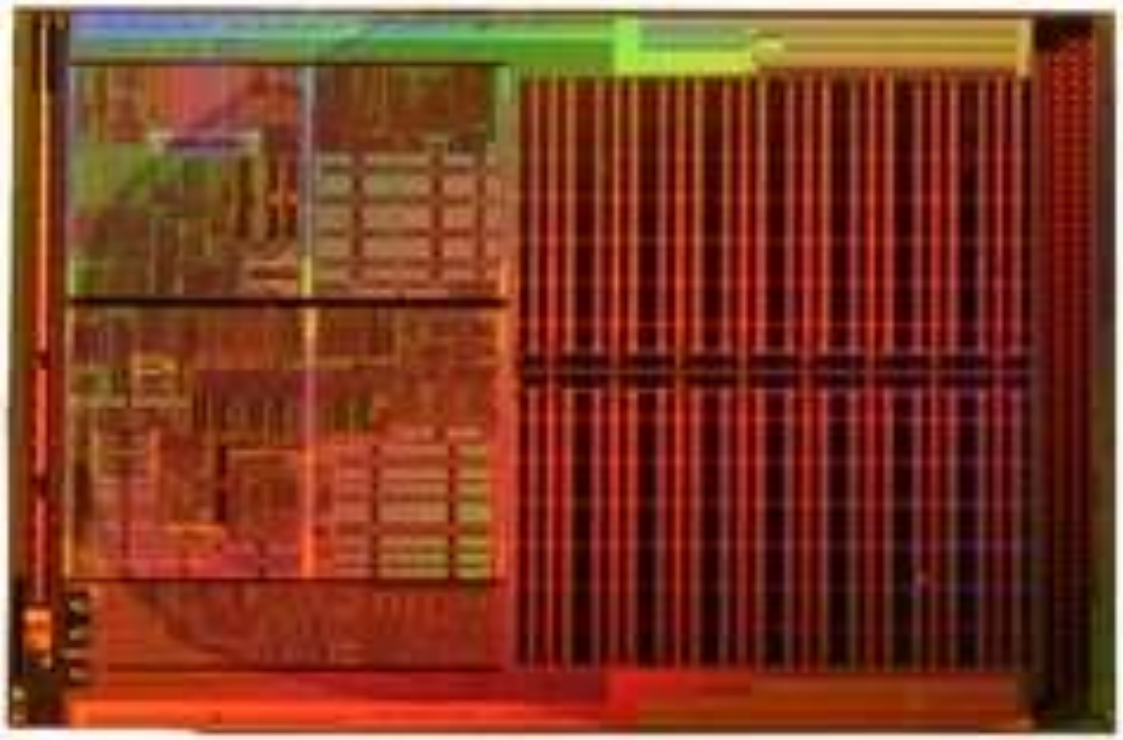


- The first Intel® Pentium® M processor, the Intel® 855 chipset family, and the Intel® PRO/Wireless 2100 network connection are the three components of Intel® Centrino™ mobile technology. Intel Centrino mobile technology is designed specifically for portable computing, with built-in wireless LAN capability and breakthrough mobile performance. It enables extended battery life and thinner, lighter mobile computers.
- 12 March 2003
- 130 nm
- 1.6 GHz
- 77 million transistors
- 1 MB integrated L2 cache

The move away from core frequency begins!

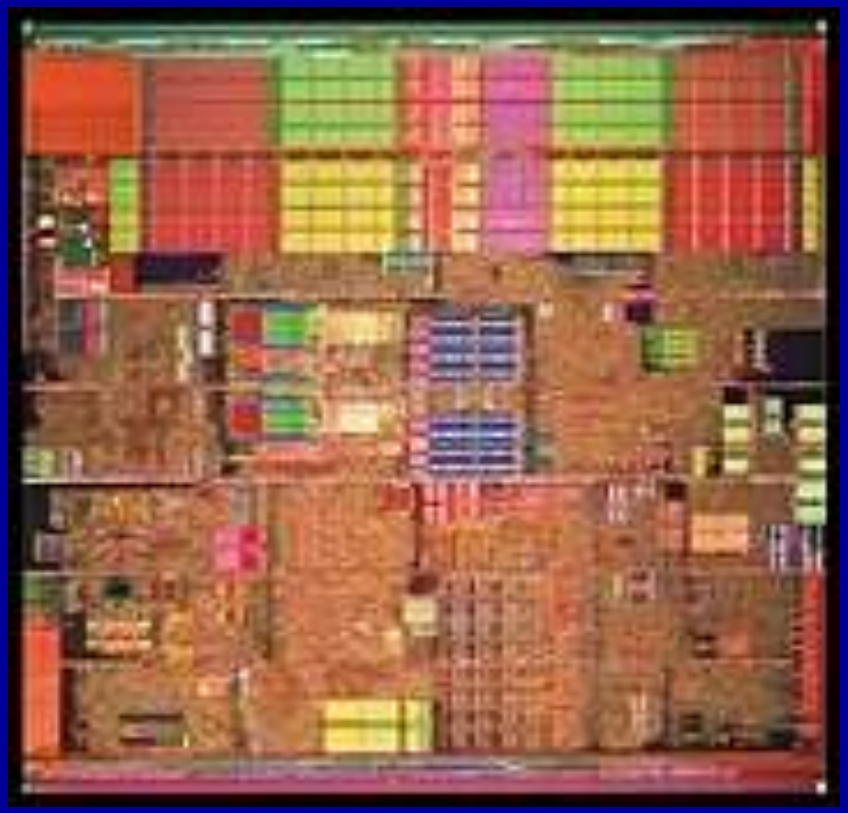
AMD Hammers Intel with AMD64





First x86 processor with 64 bits and Integrated Memory Controller

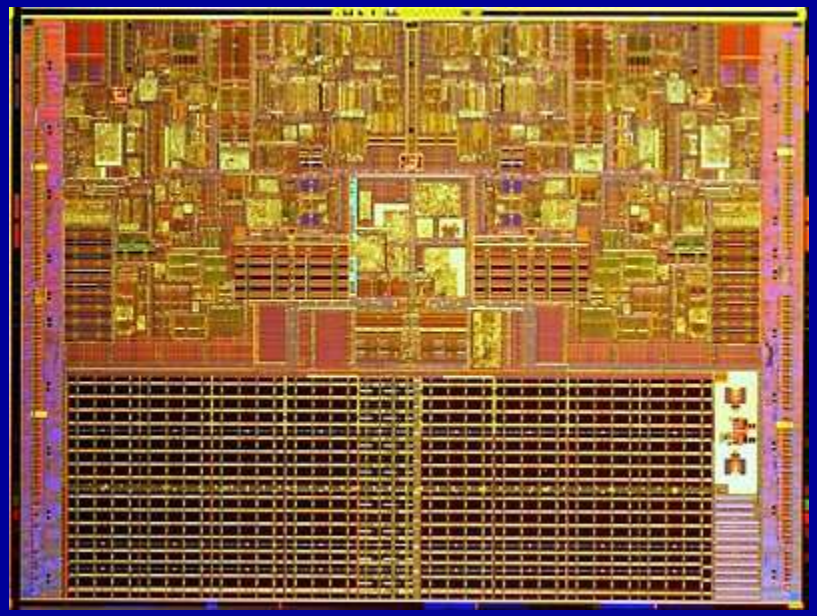
2004: Intel® Pentium® 4 Processor – 90 nm



- 1MB L2 cache
- 64-bit extensions compatible with AMD64
- 120 million transistors
- 3+ GHz frequency

intel

2006: Intel's 1st Monolithic Dual Core

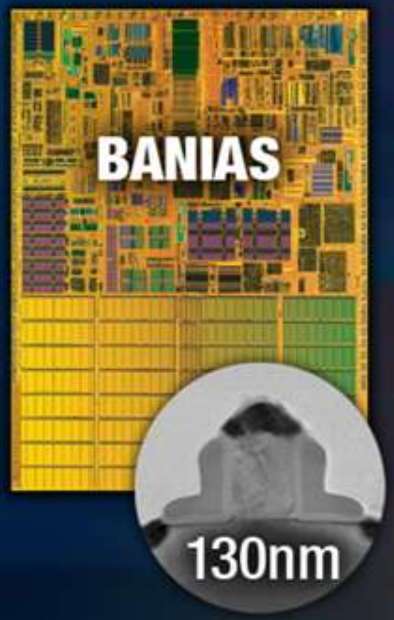


- January 2006
- **Intel® Core™ Duo Processor**
- **90 mm²**
- **151M transistors**
- **65 nm**

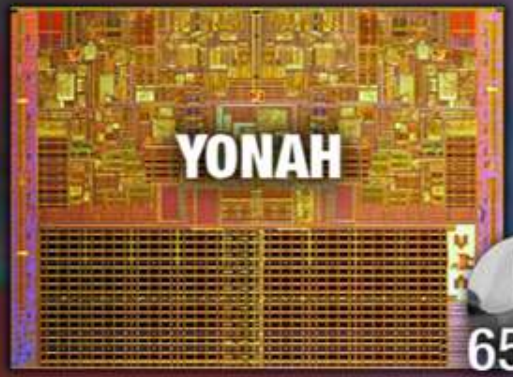
The Core Duo is also famous for being the first Intel processor to ever be used in Apple Macintosh Computers

intel

2003 2004 2006 July 27, 2006

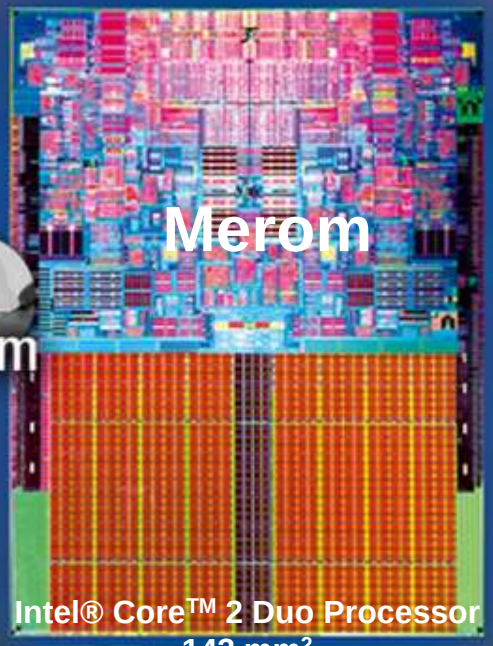


Tick



Intel® Core™ Duo Processor
90 mm²
151M transistors

Tock



Intel® Core™ 2 Duo Processor
143 mm²
291M transistors

Banias was initially planned as Celeron, but was elevated to Mainstream Mobile in 2000 as part of Centrino brand.

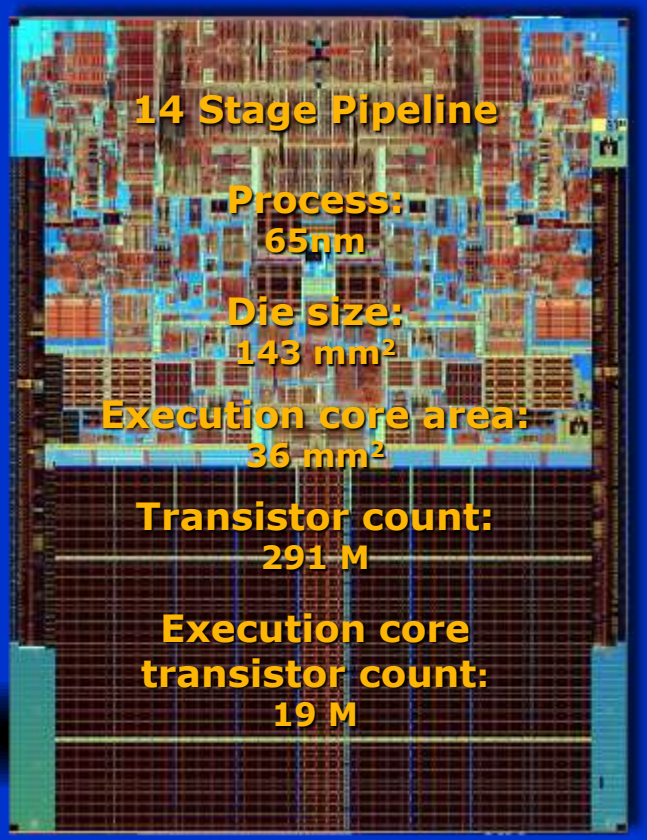
Intel® Core™ Microarchitecture

- **Intel® Wide Dynamic Execution**
- **Intel® Advanced Digital Media Boost**
- **Intel® Advanced Smart Cache**
- **Intel® Smart Memory Access**
- **Intel® Intelligent Power Capability**
- **Intel® 64 Architecture (Not IA-64)**

intel

2006: Intel® Core™ Micro-architecture Products

- Intel® Wide Dynamic Execution
- Intel® Intelligent Power Capability
- Intel® Advanced Smart Cache
- Intel® Smart Memory Access
- Intel® Advanced Digital Media Boost



Server

Desktop

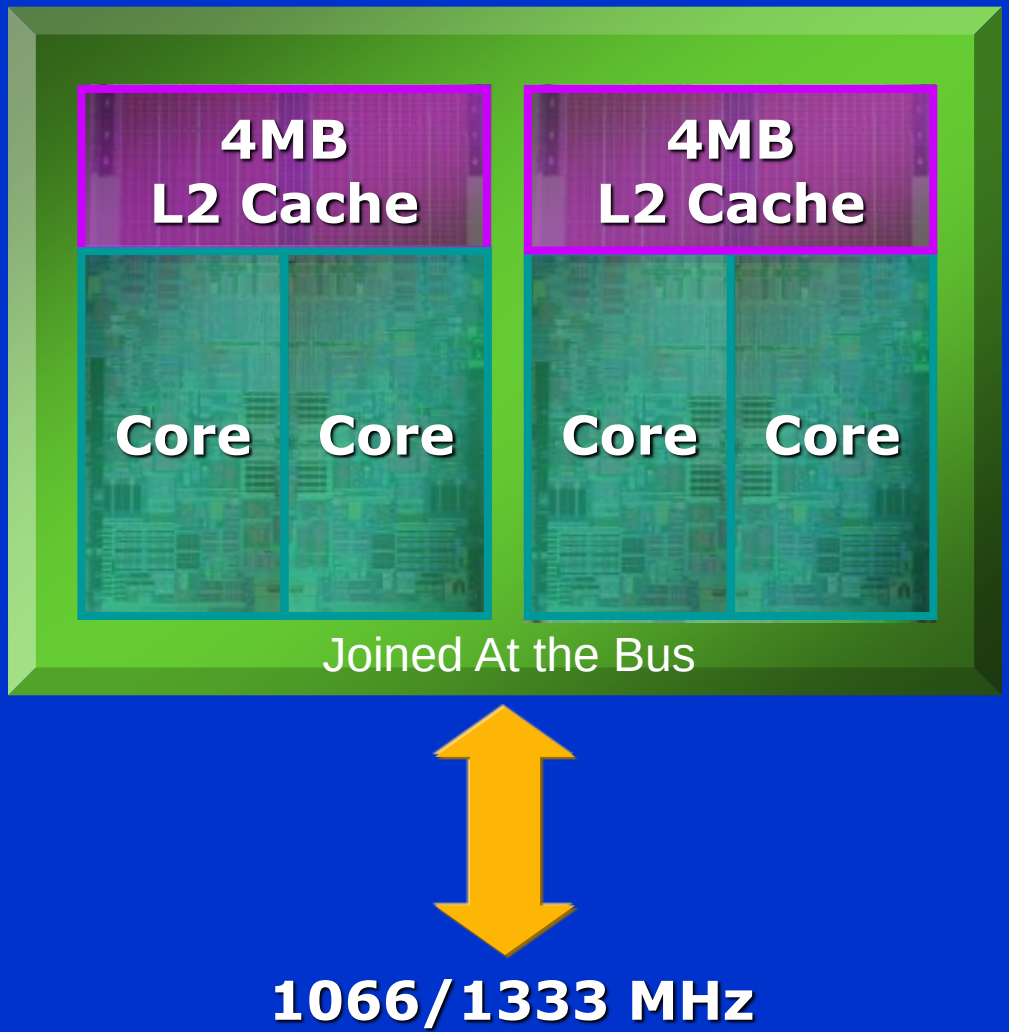
Mobile

The Empire Strikes Back!

Thanks to Israel Design Center!

intel

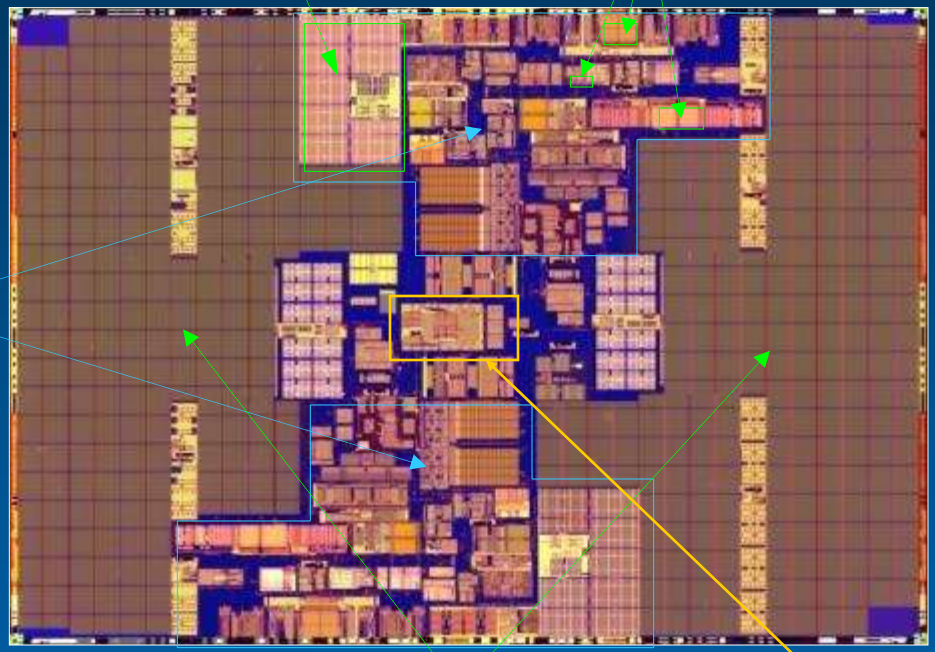
October 2006: The World's First x86 Quad-Core Processor



intel

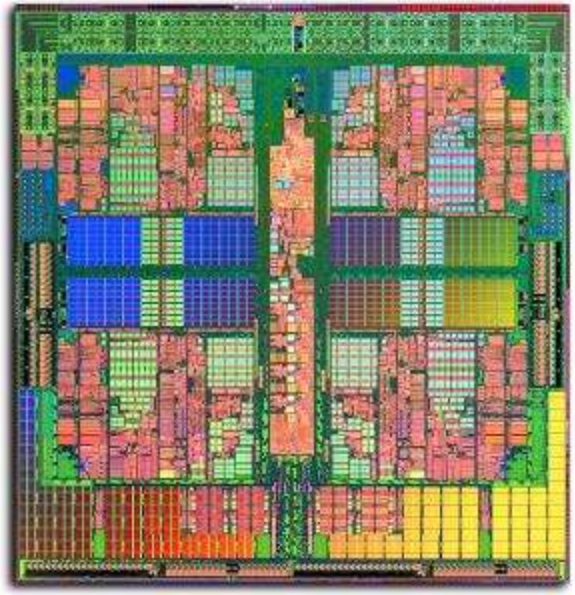
Montecito

2006: Itanium 2: First Billion Transistor Dual Core Chip (90nm)

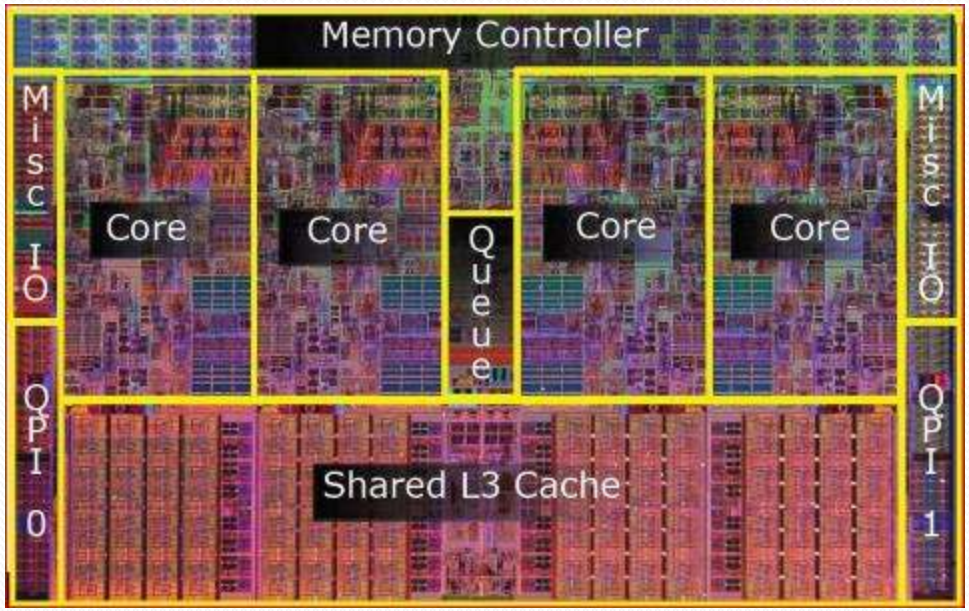


1.72 Billion Transistors (596 mm²)

2008: Performance Race Gets Serious With Quad Core



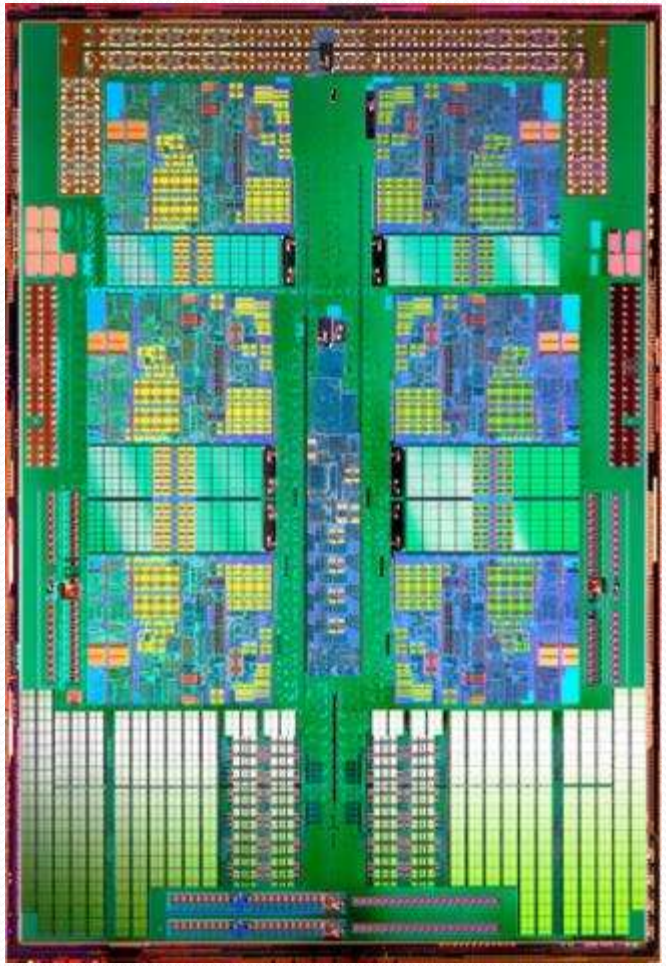
AMD Barcelona



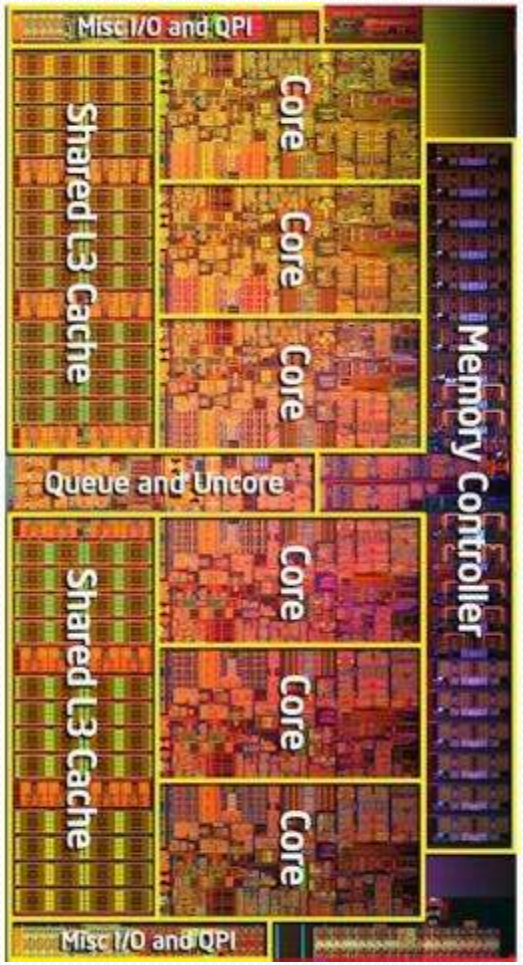
Intel Nehalem

Intel finally integrates Memory Controller

Six Cores



2009: AMD Istanbul



2010: Intel Westmere

Moore's Law Enables Microprocessor Advances

Chatting with Gordon Moore
http://www.youtube.com/watch?v=xzxpO0N5Amc

1.0µm 0.8µm 0.6µm 0.35µm 0.25µm 0.18µm 0.13µm 90nm 65nm

Intel 486™ Processor


Pentium® Processor




Pentium® II/III Processor




Pentium® 4 Processor



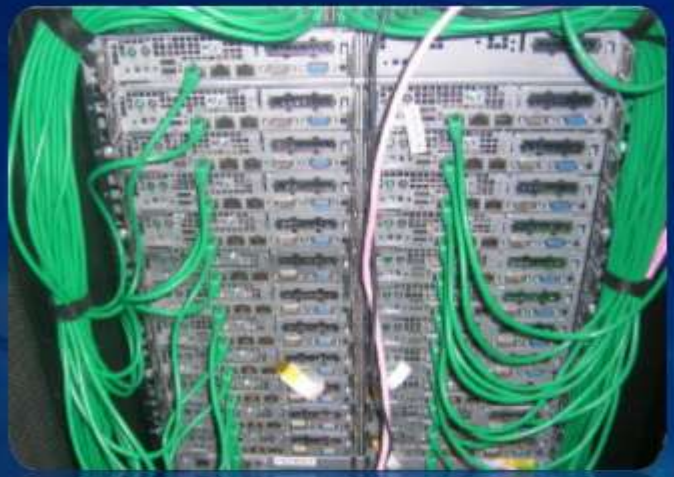
Intel® Core™ Duo Processor

Intel® Core™ 2 Duo Processor

Source: Intel

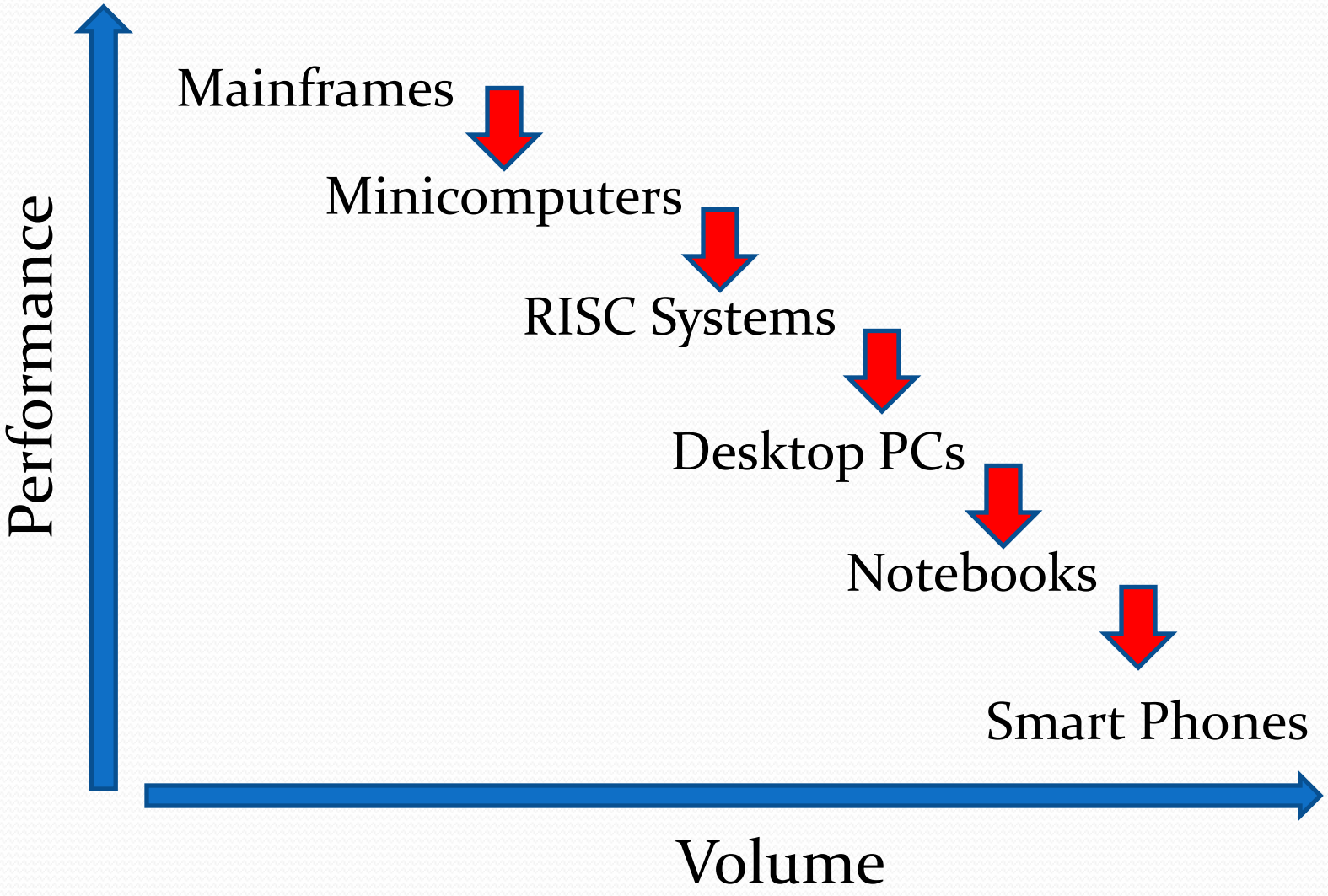
Data Centers at Microsoft

Cloud Optimized High Density Servers



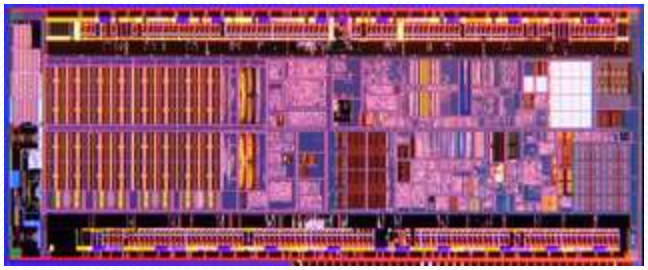
Servers built using commodity components (Low Power 2 socket CPUs, SATA HDD, MLC SSD)
No redundancy features in hardware (e.g. RAID, dual Power Supplies)
Applications specifically designed to provide Resiliency and Fault Tolerance

Disruptions Come from Below!



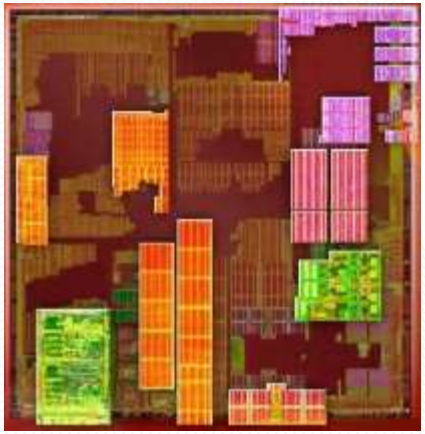
Era of Small Cores

- Intel Atom



- AMD Bobcat

- ARM



The Smart Phone Era Is Redefining Computing

Smartphones are changing consumer behavior

Result of immediacy, portability, and connectedness

70+%
Can't leave the home without it

~80%
Play games on their phones

~90%
Use their phones to search and shop

~80%
Use phones to navigate

~60%
Access their Facebook site via mobile phone

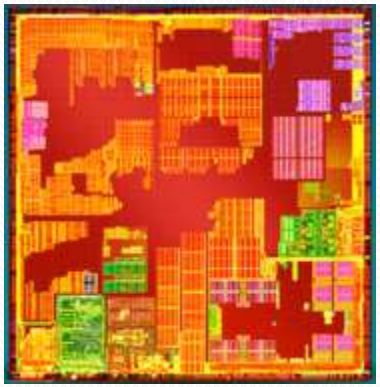
1B
Access social networks via mobile

~1/3
Watch movies on their device

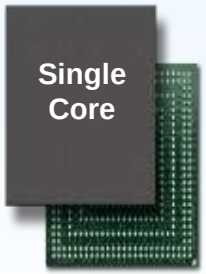
~80%
Take pictures with mobile device instead of traditional camera

Sources: Facebook, Jan. '13; SA, Apr.'12; 2012 Snapdragon Consumer Survey; TIME Mobility Poll, in cooperation with QUALCOMM, Aug. '12

Qualcomm Processor Portfolio

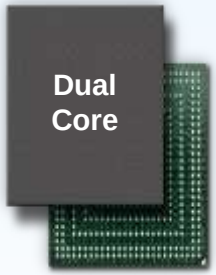


Q4 2011



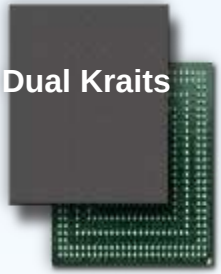
First 1GHz Single Core

Q2 2012

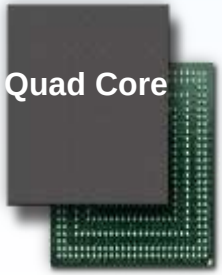


Dual Core

Q1 2013



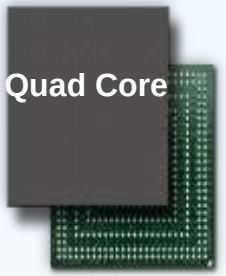
- Dual "Krait" CPUs
- Adreno GPU
- 28nm process
- Faster memory
- Industry leading modem
- Integrated Connectivity
- GPS



Quad Core

- Quad Core A5 CPUs
- Adreno GPU
- LPDDR2
- DSDS and DSDA
- 720p capture and playback
- Up to 8 Megapixel camera

Q3 2013

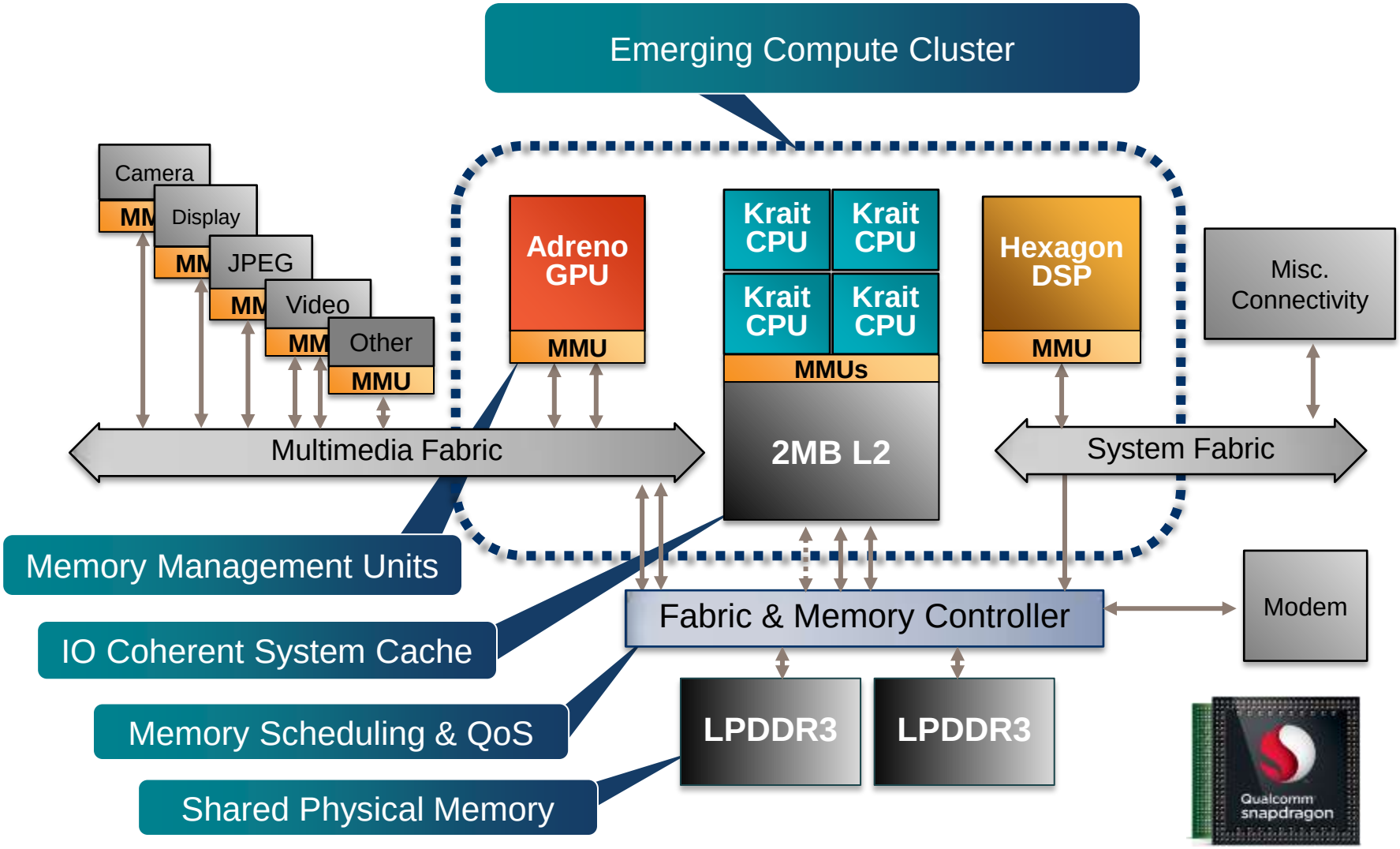


Newest Quad Core

- Quad Core A7 CPUs
- Adreno GPU
- TDSCDMA, HSPA+
- DSDS and DSDA
- 1080p capture and playback
- Up to 13 megapixel camera

Qualcomm snapdragon

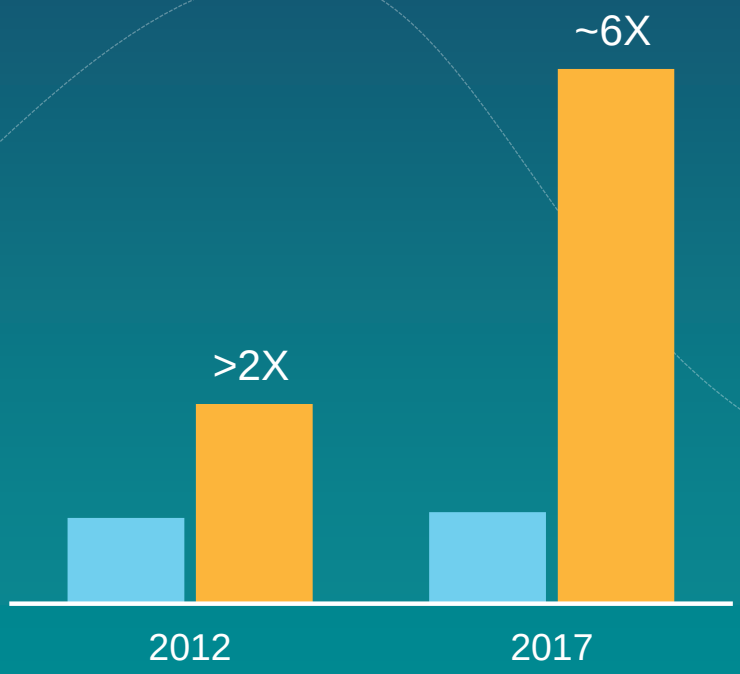
Evolving the System Architecture



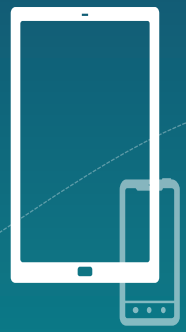
Snapdragon 800

A new era: mobile drives growth and innovation in computing

Device shipments



Semiconductor revenues



$51B — 2012 — $68B

$56B — 2016 — $90B

PCs

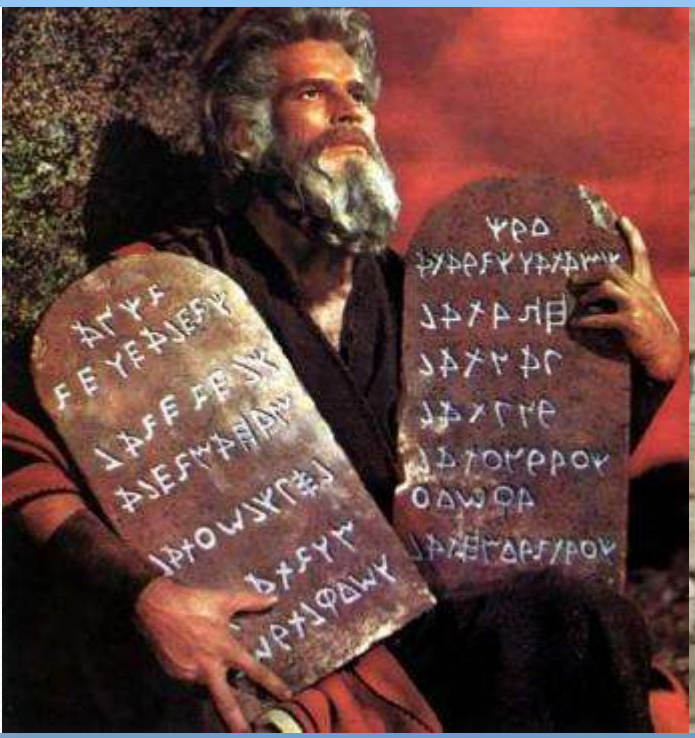
Mobile devices

Source: Smartphones units: Gartner, Mar-13; Tablet units: Avg of Gartner, Mar-13 & SA, Apr-13; PC units (desktop + portable): Avg of Gartner, Mar-13 & IDC, Feb13; Semiconductor revenue: Gartner, Dec. '12; Mobile devices include mobile phones and tablets.

Learn to wear Many Hats!

“Don’t be encumbered by past history, go off and do something wonderful.”

Shalom!



Abstract

- I had the privilege of being the first speaker at the First Annual Symposium on Computer Architecture in 1973. Over the last 40 years I have worked on PDP-11, VAX, MIPS, Alpha, x86, Itanium, and ARM processors and systems.
- Moore's Law has enabled computer architects to increase the pace of innovation and the development of microprocessors with new instruction sets.
- In the 1970s, minicomputers from Digital Equipment Corporation, Data General and Hewlett Packard started to challenge IBM mainframes. The introduction of the 32-bit VAX-11/780 in 1978 was a landmark event. The single chip MicroVAX was introduced in 1985.
- The IBM PC was introduced on August 12, 1981, followed by many IBM PC compatible machines from Compaq and others. This led to the tremendous growth of x86 processors from Intel and AMD. Today, the x86 processor dominate the computer industry.
- In 1987, the introduction of RISC processors based on Sun's SPARC architecture spawned the now famous RISC vs CISC debates. RISC processors from MIPS, IBM (Power, Power PC), and HP (PA-RISC) started to gain market share. This forced Digital to first adopt MIPS processors, and later introduce Alpha in 1992.
- The RISC supremacy continued until the introduction of the first out of order x86 Pentium Pro processor in 1995, expanding the role of x86 into workstations and servers. The x86 architecture was extended to 64 bits by AMD in the Opteron processor in 2003, forcing Intel to launch its own compatible processor.
- Disruptive technologies usually come from below. We have seen users migrate from mainframes to minicomputers to RISC workstations and servers to desktop PCs and PC servers to notebooks and tablets. Volume economics has driven the industry. The next wave will be the technology used in smart phones. With over a billion chips sold annually, this technology will appear in other platforms. Several companies have announced plans for ARM based servers.
- Moore's Law has also enabled computer architects to advance the sophistication of microprocessors. We will review some of the significant milestones leading from the first Intel 4004 to today's state of the art processors.